TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

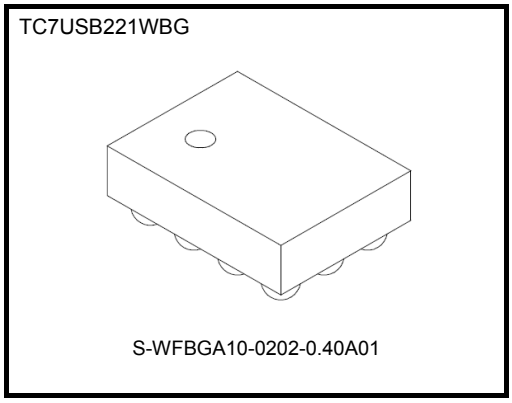
TC7USB221WBG

Dual SPDT USB Switch

TC7USB221 is high-speed CMOS dual 1-2 multiplexer /demultiplexer. The low ON-resistance and the low capacitance of the switch allow connections to USB application.

This device consists of dual individual two-inputs multiplexer/demultiplexer with common select input (S) and output enable ($\overline{OE}$). The D+/D- inputs is connected to the D1+/D1- or D2+/D2- outputs determined by the combination both the select input (S) and output enable ($\overline{OE}$). When the output enable ($\overline{OE}$) input is held "H" level, the switches are open with regardless the state of select inputs and a high-impedance state exists between the switches.

All inputs are equipped with protection circuits against static discharge.



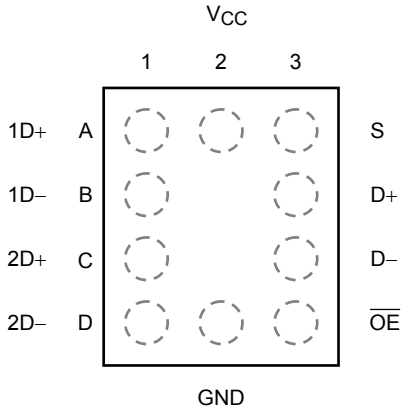
Weight
S-WFBGA10-0202-0.40A01 : 0.0025 g (typ.)

Features

- Operating voltage: V_{CC} = 2.3 to 3.6 V
- ON-capacitance: $C_{I/O}$ = 7 pF Switch ON(typ.)@V_{CC}=3.3 V
- ON-resistance: R_{ON} = 6.5 Ω (typ.)@V_{CC}=3 V, $V_{I/O}$=0 V
- R_{ON} Flatness: $R_{ON(flat)}$ = 1.6 Ω (typ.)@V_{CC}=3 V
- Delta R_{ON}: ΔR_{ON} = 0.5 Ω (typ.)@V_{CC}=3 V
- ESD performance: Machine model ≥ ± 200 V
  Human body model ≥ ± 2000 V
- Power-down protection for inputs ($\overline{OE}$ and S, I/O)
- Package : WCSP10

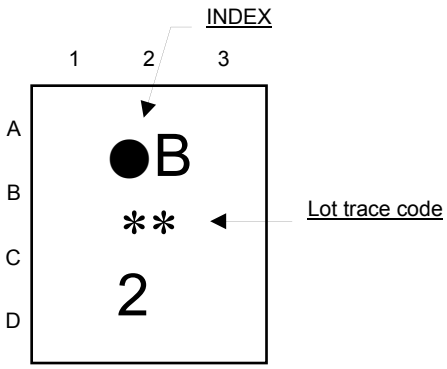
Pin Assignment (top view)

WBG (S-WFBGA10-0202-0.40A01)



Marking

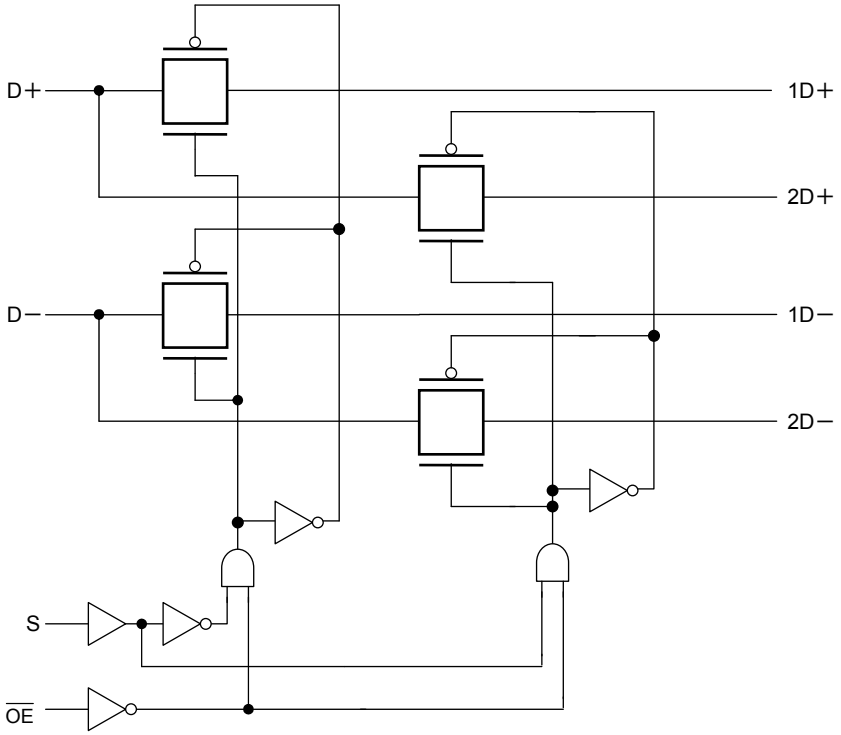
WBG (S-WFBGA10-0202-0.40A01)



Truth Table

Inputs		Function
$\overline{OE}$	S	
L	L	D+ port = 1D+ port, D- Port = 1D- Port
L	H	D+ port = 2D+ port, D- Port = 2D- Port
H	X	Disconnect

System Diagram



Absolute Maximum Ratings (Note)

Characteristic		Symbol	Rating	Unit
Power supply range		V_{CC}	−0.5 to 4.6	V
Control pin input voltage ($\overline{OE}$, S)		V_{IN}	−0.5 to 4.6	V
Switch terminal I/O voltage	V_{CC}=0 V or Switch=Off	V_S	−0.5 to 4.6	V
	Switch=On		−0.5 to V_{CC}+0.5	
Clump diode current	Control input	I_{IK}	−50	mA
	Switch		±50	
Switch I/O current		I_S	50	mA
Power dissipation		P_D	150	mW
DC V_{CC}/GND current		I_{CC}/I_{GND}	±100	mA
Storage temperature		T_{stg}	−65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction. Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristic		Symbol	Rating	Unit
Power supply voltage		V_{CC}	2.3 to 3.6	V
Control pin input voltage ($\overline{OE}$, S)		V_{IN}	0 to 3.6	V
Switch I/O voltage	V_{CC}=0 V or Switch=Off	V_S	0 to 3.6	V
	Switch=On		0 to V_{CC}	
Operating temperature		T_{opr}	−40 to 85	°C
Input rise and fall time		dt/dv	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics (Ta = –40 to 85°C)

Characteristics		Symbol	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit
Input voltage ($\overline{OE}$, S)	"H" level	V_{IH}	—	2.3 to 3.6	0.46 × V_{CC}	—	—	V
	"L" level	V_{IL}	—	2.3 to 3.6	—	—	0.25 × V_{CC}	
Input leakage current ($\overline{OE}$, S)		I_{IN}	V_{IN} = 0 to 3.6 V	2.3 to 3.6	—	—	±1.0	μA
Power-off leakage current		I_{OFF}	V_{IN} = 0 to 3.6 V	0	—	—	±5.0	μA
Off-state leakage current (switch off)		I_{SZ}	D+, D- = 0 to V_{CC}, $\overline{OE}$ = V_{CC}	2.3 to 3.6	—	—	±5.0	μA
ON resistance (Note2)		R_{ON}	V_{IS} = 0 V, I_{IS} = 30 mA (Note1)	3.0	—	6.5	10	Ω
			V_{IS} = 0.4 V, I_{IS} = 30 mA (Note1)	3.0	—	7	11	
			V_{IS} = 3.0 V, I_{IS} = 30 mA (Note1)	3.0	—	13	19	
Delta R_{ON}		ΔR_{ON}	V_{IS} = 0.4 V, 1.0V, I_{IS} = 30 mA	3.0	—	0.5	—	Ω
On-Resistance Flatness		$R_{ON(flat)}$	V_{IN} = 0V to 1.0V, I_{IS} = 30 mA	3.0	—	1.6	—	Ω
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0	3.6	—	—	2.0	μA
Increase in I_{CC} per input		ΔI_{CC}	V_{IN} = 1.8V	3.6	—	—	10.0	μA

Note1: All typical values are at Ta = 25°C.

Note2: Measured by the voltage drop between D+/D- and D1+/D1-, D2+/D1- pins at the indicated current through the switch. ON resistance is determined by the lower of the voltages on the two pins.

AC Characteristics V_{CC}=3.3V± 10% (Ta = –40 to 85°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit
Propagation Delay Time (Note)	tpd	C_L=5 pF	3.3 ± 0.3	—	0.25	—	ns
Turn ON Time (S, $\overline{OE}$ to Output)	t_{ON}	R_L=50 Ω, C_L=5 pF	3.3 ± 0.3	—	7.5	17	ns
Turn OFF Time (S, $\overline{OE}$ to Output)	t_{OFF}	R_L=50 Ω, C_L=5 pF	3.3 ± 0.3	—	3.3	10	ns
Break Before Make	TBBM	R_L=50 Ω, C_L=5 pF	3.3 ± 0.3	2	—	7.0	ns
Output skew between center port to any other port (Note)	$t_{SK(O)}$	C_L=5 pF	3.3 ± 0.3	—	0.1	—	ns
Skew of Opposite Transitions of the same output (tp_{HL}- tp_{LH}) (Note)	$t_{SK(P)}$	C_L=5 pF	3.3 ± 0.3	—	0.1	—	ns
Off Isolation (Non-Adjacent)	OIRR	R_T=50 Ω, f=240 MHz	3.3 ± 0.3	—	-36	—	dB
Crosstalk(Non-Adjacent)	XTalk	R_T=50 Ω, f=240 MHz	3.3 ± 0.3	—	-36	—	dB
-3dB Bandwidth	BW	R_T=50 Ω,C_L=0 pF	3.3 ± 0.3	—	820	—	MHz

Note: This parameter is guaranteed by design.

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Control pin input capaci tance ($\overline{OE}$, S)	C_{IN}	V_{IN} = 0 V (Note)	3.3	4	pF
Switch terminal Off capacitance (D+, D−)	$C_{I/O}$	V_{IS} = 0 V, $\overline{OE}$ = V_{CC} (Note)	3.3	4	pF
Switch terminal Off capacitance (1D+, 1D−, 2D+, 2D−)	$C_{I/O}$	V_{IS} = 0 V, $\overline{OE}$ = V_{CC} (Note)	3.3	3	pF
Switch terminal On capacitance	$C_{I/O}$	V_{IS} = 0 V, $\overline{OE}$ = GND (Note)	3.3	7	pF

Note: This parameter is guaranteed by design.

AC Test Circuit Load/Waveform

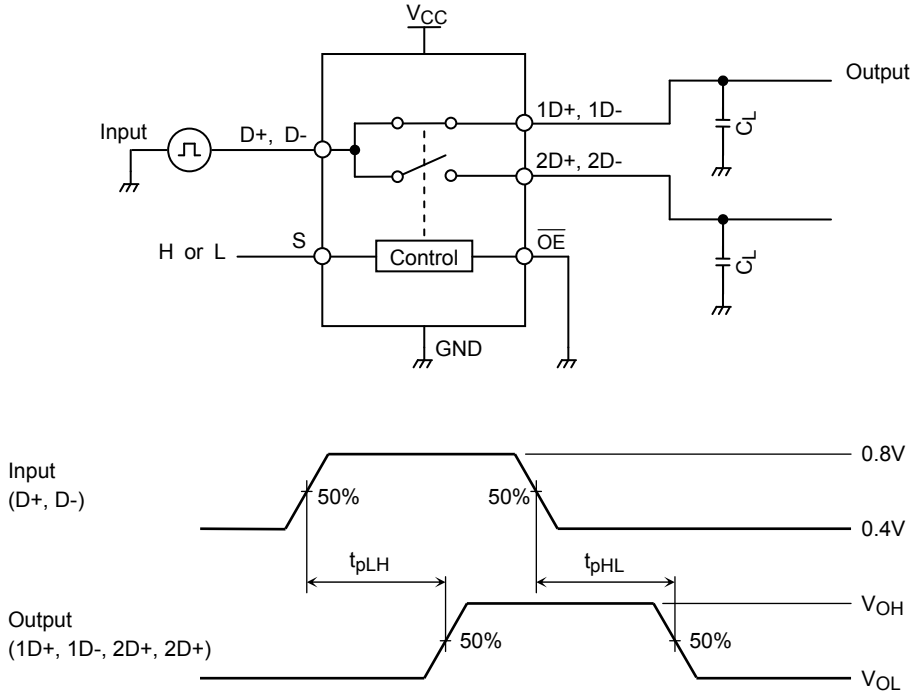


Figure 1 : Propagation Delay Time (t_{pLH}, t_{pHL})

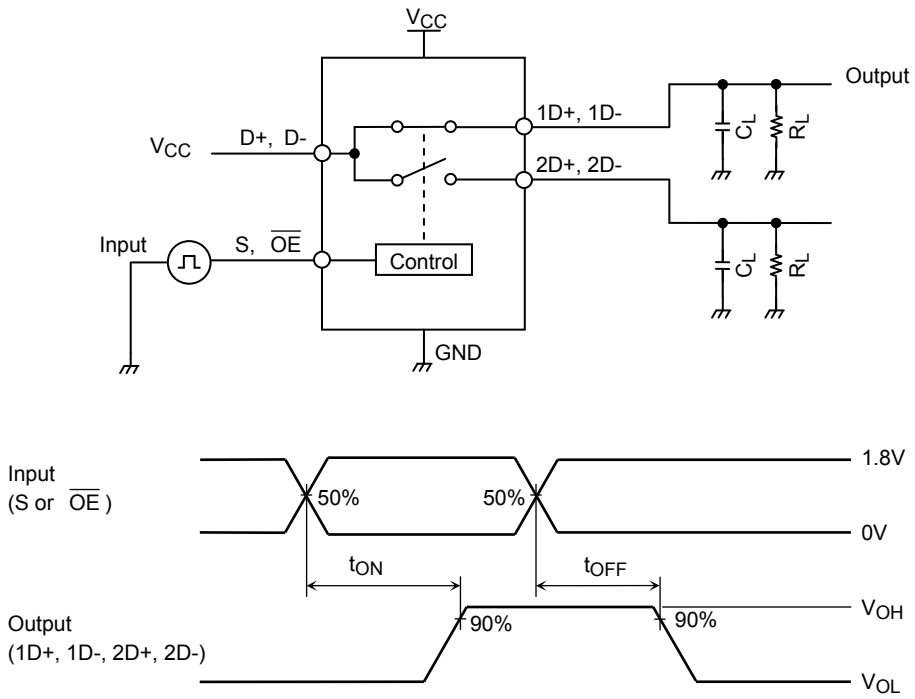


Figure 2 : Turn ON/Turn OFF (t_{ON}, t_{OFF})

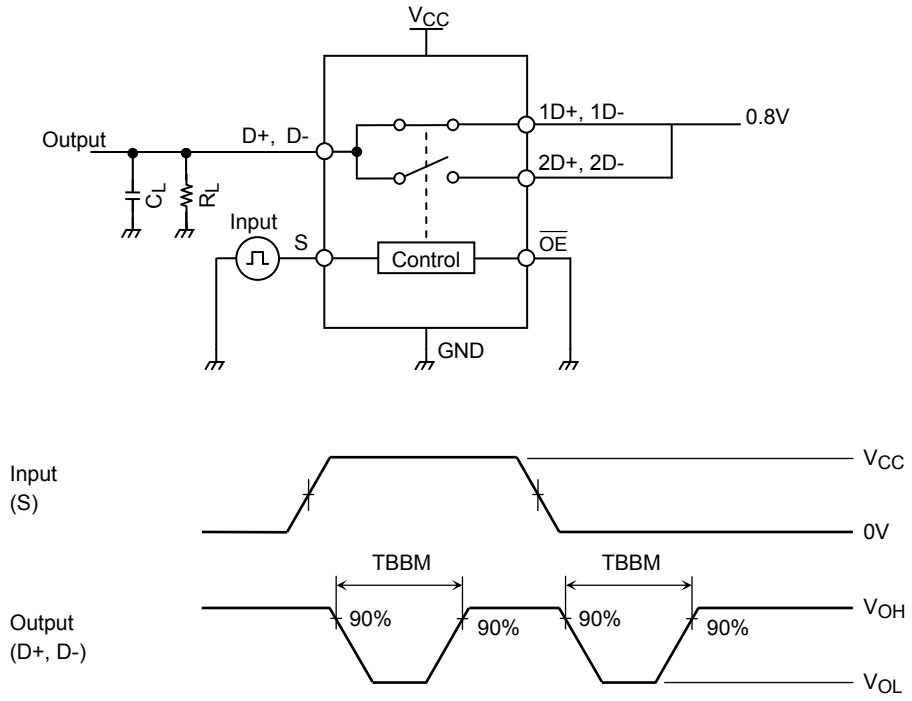
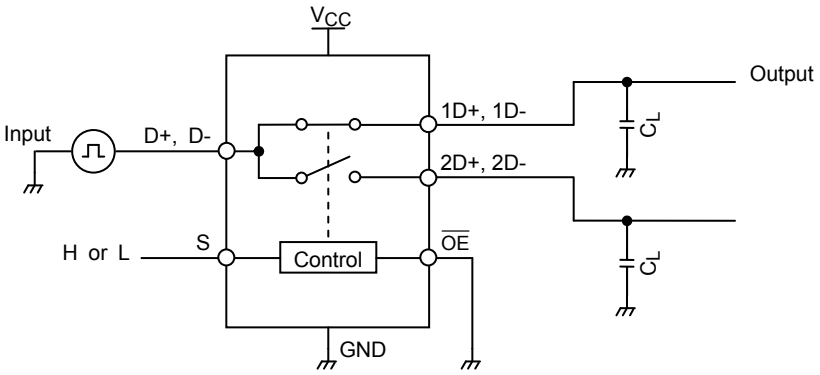
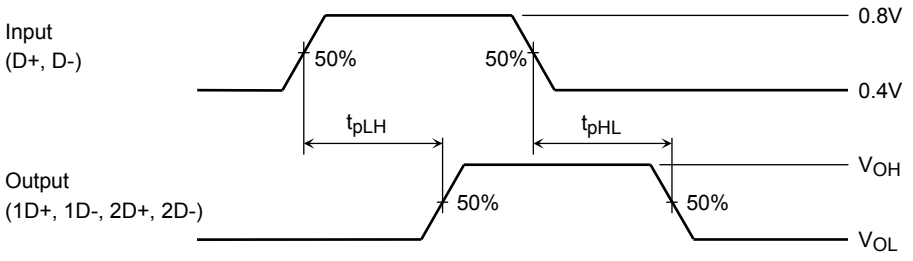
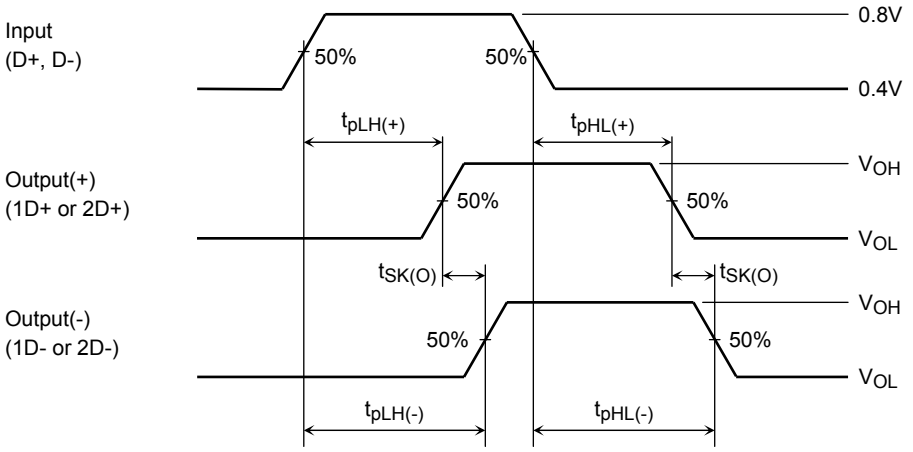


Figure 3 : Break Before Make (TBBM)





PULSE SKEW $t_{SK(P)} = |t_{pLH} - t_{pHL}|$



OUTPUT SKEW $t_{SK(O)} = |t_{pLH(+)} - t_{pLH(-)}|$ **or** $|t_{pHL(+)} - t_{pHL(-)}|$

Figure 4 : Skew of Opposite Transitions of the same output, Output skew

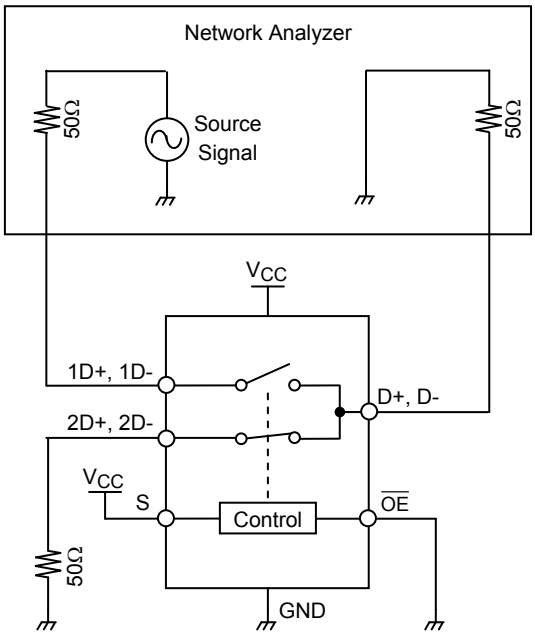


Figure 5 : Channel OFF Isolation

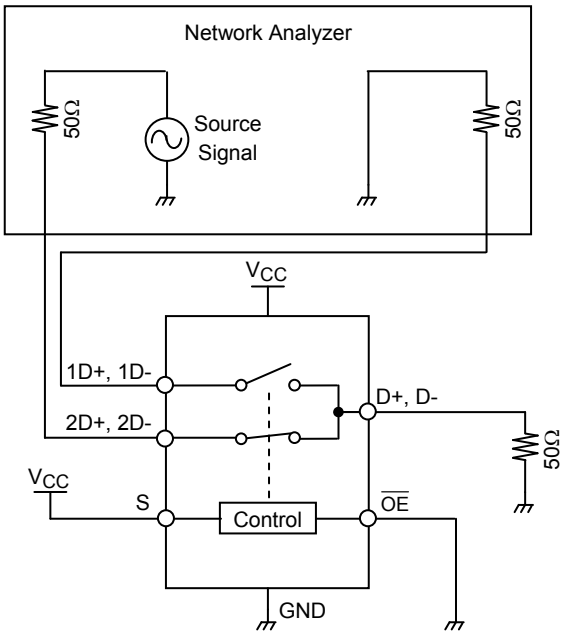


Figure 6 : Crosstalk

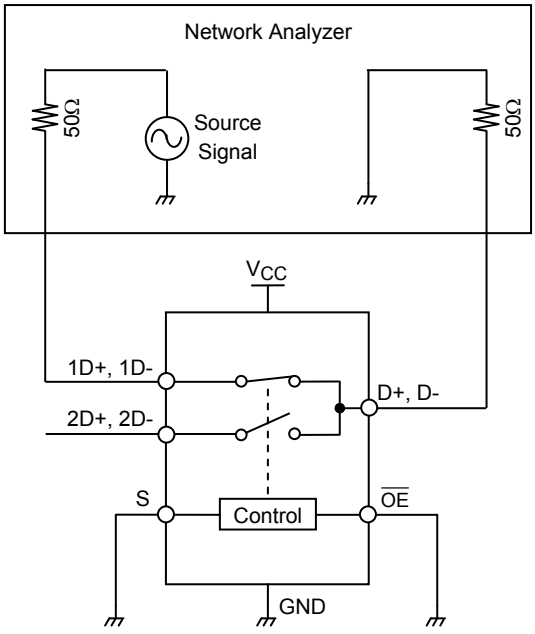


Figure 7 : -3dB Bandwidth

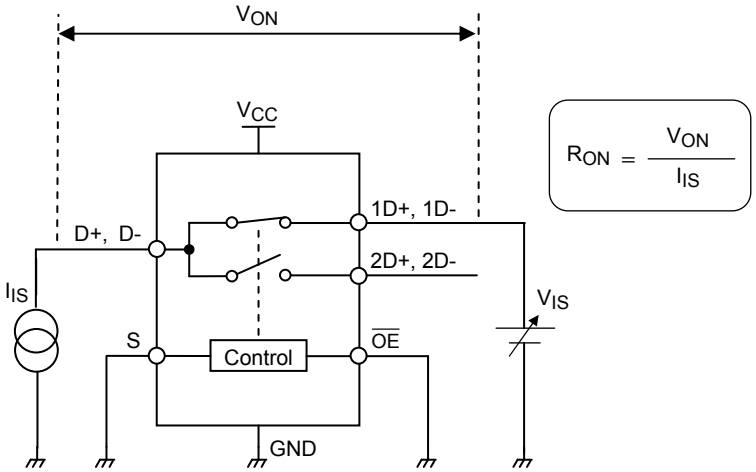


Figure 8 : ON Resistance

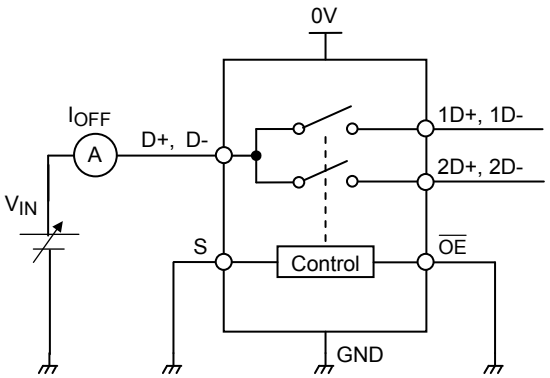


Figure 9 : Power off Leakage Current

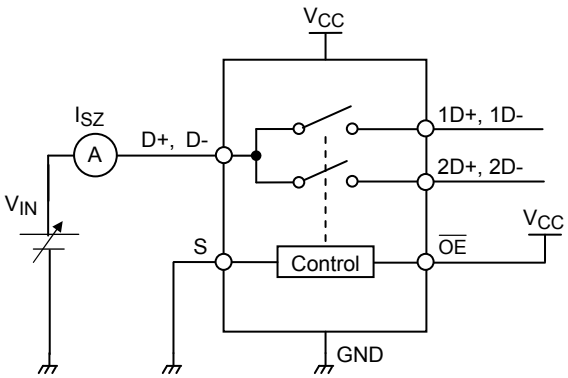
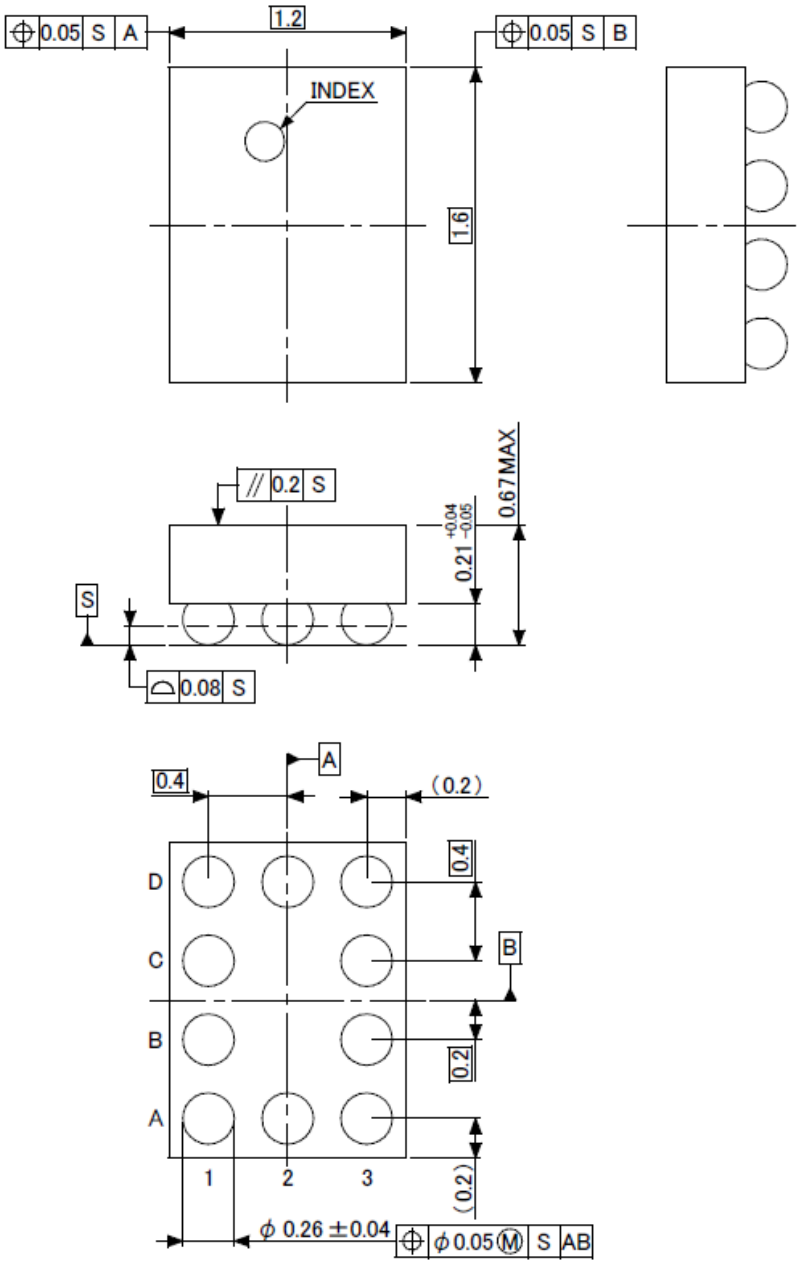


Figure 10 : Off-State Leakage current

Package Dimension

S-WFBGA10-0202-0.40A01 Unit: mm



The resin used in this product includes no flame retardants.

Weight: 0.0025g (Typ.)

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