TK100A08N1

This material is for a technological examination material to aim at the product introduction. The change in the content of the characteristic might be accompanied at the final specification process. The latest specification will be able to be gotten in the brokerage department when the product of an equipment is designed and to get the confirmation.

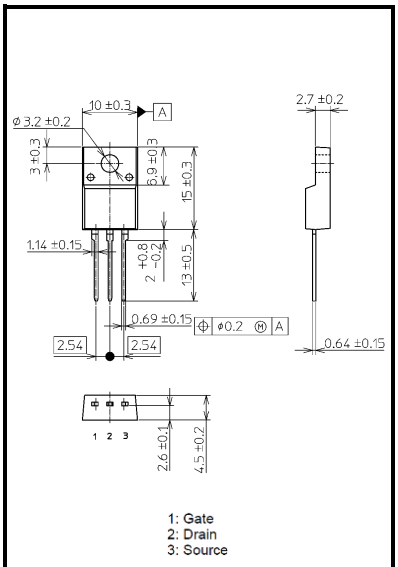
TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type (U-MOSⅧ-H)

TK100A08N1

Switching Regulator Applications

- Low drain-source on-resistance:
  $R_{DS(ON)}$ = 2.6 mΩ (typ.) (V_{GS} = 10 V)
- Low leakage current: I_{DSS} = 10 μA (max) (V_{DS} = 80 V)
- Enhancement mode: V_{th} = 2.0 to 4.0 V (V_{DS} = 10 V, I_D = 1.0 mA)

Unit: mm



JEDEC	―
JEITA	SC-67
TOSHIBA	2-10U1S

Weight: 1.7 g (typ.)

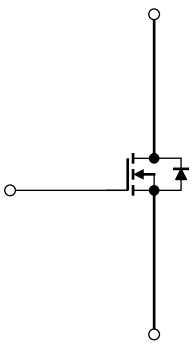
Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	80	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC(Silicon limit)(Note 1,2)	I_D	214	A
	DC(Tc=25℃)(Note 1)	I_D	100	
	Pulsed(t=1ms)(Note 1)	I_{DP}	568	
Drain power dissipation (T_c = 25°C)		P_D	45	W
Single-pulse avalanche energy (Note 3)		E_{AS}	278	mJ
Avalanche current		I_{AR}	100	A
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristic	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	2.77	°C/W
Thermal resistance, channel to ambient	$R_{th(ch-a)}$	62.5	°C/W



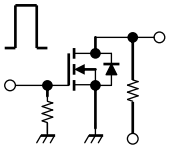
Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: Limited by silicon capability. Package limit is 100A.

Note 3: V_{DD} = 64 V, T_{ch} = 25°C (initial), L = 21.4 μH, R_G = 1.2 Ω, I_{AR} = 100 A

This transistor is an electrostatic-sensitive device.
Please handle with caution.

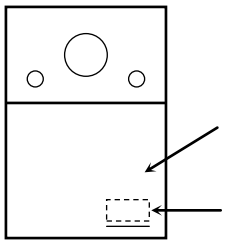
Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	—	—	±0.1	μA
Drain cutoff current		I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V	—	—	10	μA
Drain-source breakdown voltage		$V_{(BR)DSS}$	I_D = 10 mA, V_{GS} = 0 V	80	—	—	V
		$V_{(BR)DSX}$	I_D = 10 mA, V_{GS} = −20 V (Note 4)	52	—	—	
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1.0 mA	2.0	—	4.0	V
Drain-source on-resistance		$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 50 A	—	2.6	3.2	mΩ
Input capacitance		C_{iss}	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz	—	9100	—	pF
Reverse transfer capacitance		C_{rss}		—	40	—	
Output capacitance		C_{oss}		—	2400	—	
Gate resistance		rg		—	2.8	—	Ω
Switching time	Rise time	t_r		—	26	—	ns
	Turn-on time	t_{on}		—	53	—	
	Fall time	t_f		—	46	—	
	Turn-off time	t_{off}	Duty ≤ 1%, t_w = 10 μs	—	140	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≈ 64 V, V_{GS} = 10 V, I_D = 100 A	—	130	—	nC
Gate-source charge 1		Q_{gs1}		—	45	—	
Gate-drain (“Miller”) charge		Q_{gd}		—	33	—	
Gate switch charge		Q_{SW}		—	53	—	

Source−Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	100	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	568	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 100 A, V_{GS} = 0 V	—	—	−1.2	V
Reverse recovery time(Note 5)	t_{rr}	I_{DR} = 100 A, V_{GS} = 0 V, $-dI_{DR}$ / dt = 100 A / μs	—	93	—	ns
Reverse recovery charge(Note 5)	Q_{rr}		—	190	—	nC

Marking



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