

Memory FRAM

4 M (256 K × 16) Bit

MB85R4M2T

■ DESCRIPTIONS

The MB85R4M2T is an FRAM (Ferroelectric Random Access Memory) chip consisting of 262,144 words × 16 bits of nonvolatile memory cells fabricated using ferroelectric process and silicon gate CMOS process technologies.

The MB85R4M2T is able to retain data without using a back-up battery, as is needed for SRAM.

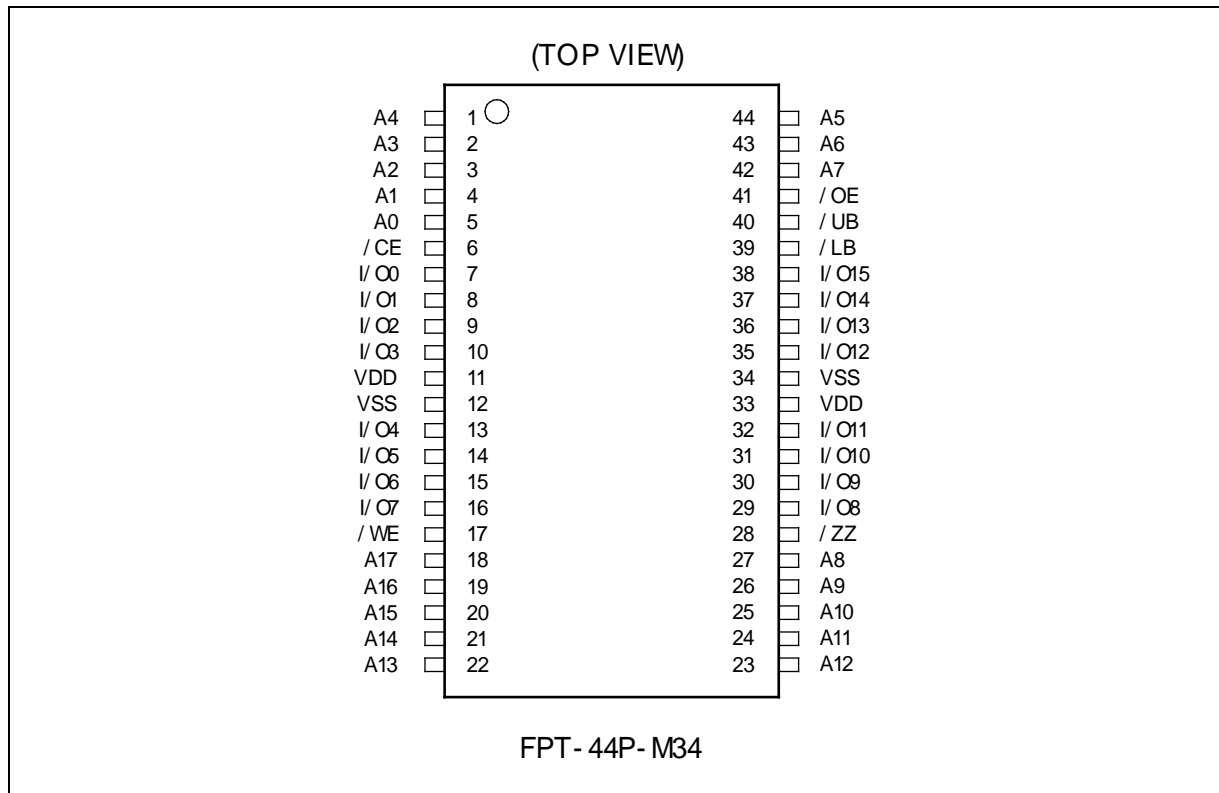
The memory cells used in the MB85R4M2T can be used for 10^{13} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E2PROM. The MB85R4M2T uses a pseudo-SRAM interface that is compatible with conventional asynchronous SRAM.

■ FEATURES

- Bit configuration : 262,144 words × 16 bits
- LB and UB data byte control : Available Configuration of 524,288 words × 8 bits
- Read/write endurance : 10^{13} times / 16 bits
- Data retention : 10 years (+ 85 °C)
- Operating power supply voltage : 1.8 V to 3.6 V
- Low power operation : Operating power supply current 20 mA (Max)
Standby current 150 μA (Max)
Sleep current 20 μA (Max)
- Operation ambient temperature range : - 40 °C to + 85 °C
- Package : 44-pin plastic TSOP (FPT-44P-M34)
RoHS compliant

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■ PIN ASSIGNMENTS



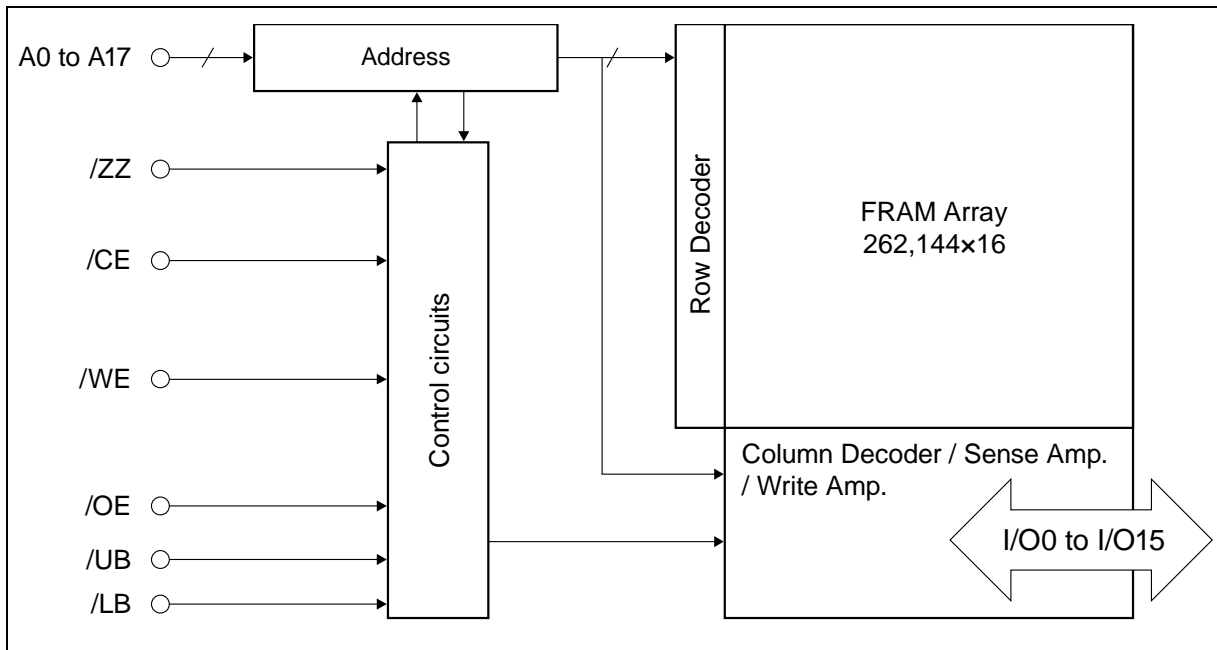
■ PIN DESCRIPTIONS

Pin Number	Pin Name	Functional Description
1 to 5, 18 to 22, 23 to 27, 42 to 44	A0 to A17	Address Input pins Select 262,144 words in FRAM memory array by 18 Address Input pins. When these address inputs are changed during /CE equals to "L" level, reading operation of data selected in the address after transition will start.
7 to 10, 13 to 16, 29 to 32, 35 to 38	I/O0 to I/O15	Data Input/Output pins These are 16 bits bidirectional pins for reading and writing.
6	/CE	Chip Enable Input pin In case the /CE equals to "L" level and /ZZ equals to "H" level, device is activated and enables to start memory access. In writing operation, input data from I/O pins are latched at the rising edge of /CE and written to FRAM memory array.
17	/WE	Write Enable Input pin Writing operation starts at the falling edge of /WE. Input data from I/O pins are latched at the rising edge of /WE and written to FRAM memory array.
41	/OE	Output Enable Input pin When the /OE is "L" level, valid data are output to data bus. When the /OE is "H" level, all I/O pins become high impedance (High-Z) state.
28	/ZZ	Sleep Mode Input pin When the /ZZ becomes to "L" level, device transits to the Sleep Mode. During reading and writing operation, /ZZ pin shall be hold "H" level.
39, 40	/LB, /UB	Lower/Upper byte Control Input pins In case /LB or /UB equals to "L" level, it enables reading/writing operation of I/O0 to I/O7 or I/O8 to I/O15 respectively. In case /LB and /UB equal to "H" level, all I/O pins become High-Z state.
11, 33	VDD	Supply Voltage pins Connect all two pins to the power supply.
12, 34	VSS	Ground pins Connect all two pins to ground.

Note: Please refer to the timing diagram for functional description of each pin.

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■ BLOCK DIAGRAM



■ FUNCTIONAL TRUTH TABLE

Operation Mode	/CE	/WE	/OE	A0 to A17	/ZZ
Sleep	×	×	×	×	L
Standby	H	×	×	×	H
Read	↓	H	L	H or L	H
Address Access Read	L	H	L	↑ or ↓	H
Write(/CE Control) ^{*1}	↓	L	×	H or L	H
Write(/WE Control) ^{*1*2}	L	↓	×	H or L	H
Address Access Write ^{*1*3}	L	↓	×	↑ or ↓	H
Pre-charge	↑	×	×	×	H

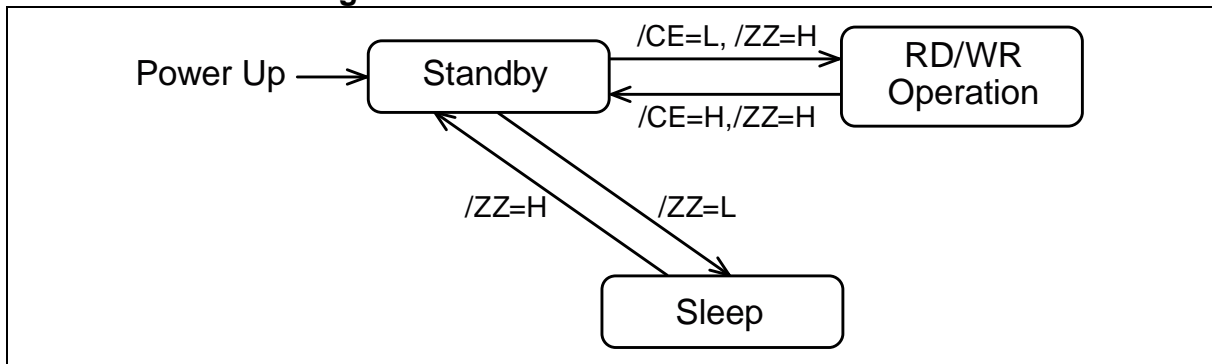
Note: H= "H" level, L= "L" level, ↑= Rising edge, ↓= Falling edge, ×= H, L, ↓ or ↑

*1: In writing cycle, input data is latched at early rising edge of /CE or /WE.

*2: In writing sequence of /WE control, there exists time with data output of reading cycle at the falling edge of /CE.

*3: In writing sequence of Address Access Write, there exists time with data output of reading cycle at the address transition.

■ State Transition Diagram



■ FUNCTIONAL TRUTH TABLE OF BYTE CONTROL

Operation Mode	/WE	/OE	/LB	/UB	I/O0 to I/O7	I/O8 to I/O15
Read(Without Output)	H	H	×	×	Hi-Z	Hi-Z
	H	×	H	H	Hi-Z	Hi-Z
Read(I/O8 to I/O15)	H	L	H	L	Hi-Z	Output
Read(I/O0 to I/O7)			L	H	Output	Hi-Z
Read(I/O0 to I/O15)			L	L	Output	Output
Write(I/O8 to I/O15)	↑	×	H	L	×	Input
Write(I/O0 to I/O7)			L	H	Input	×
Write(I/O0 to I/O15)			L	L	Input	Input

Note: H= "H" level, L= "L" level, ↑= Rising edge, ↓= Falling edge, ×= H, L, ↓ or ↑
Hi-Z= High Impedance

In case the byte reading or writing are not selected, /LB and /UB pins shall be connected to GND pin.

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■ ABABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power Supply Voltage*	V_{DD}	- 0.5	+ 4.0	V
Input Pin Voltage*	V_{IN}	- 0.5	$V_{DD} + 0.5 (\leq 4.0)$	V
Output Pin Voltage*	V_{OUT}	- 0.5	$V_{DD} + 0.5 (\leq 4.0)$	V
Operation Ambient Temperature	T_A	- 40	+ 85	°C
Storage Temperature	T_{stg}	- 55	+ 125	°C

* : All voltages are referenced to VSS (ground 0 V).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage*	V_{DD}	1.8	3.3	3.6	V
High Level Input Voltage*	V_{IH}	$V_{DD} \times 0.8$	—	$V_{DD} + 0.3$	V
Low Level Input Voltage*	V_{IL}	- 0.3	—	$V_{DD} \times 0.17$	V
Operation Ambient Temperature	T_A	- 40	—	+ 85	°C

*: All voltages are referenced to VSS (ground 0 V).

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Leakage Current	$ I_{LI} $	$V_{IN} = 0V$ to V_{DD}	—	—	5	μA
Output Leakage Current	$ I_{LO} $	$V_{OUT} = 0V$ to V_{DD} /CE = V_{IH} or /OE = V_{IH}	—	—	5	μA
Operating Power Supply Current*1	I_{DD}	/CE = 0.2 V, $I_{out} = 0$ mA	—	15	20	mA
Standby Current	I_{SB}	/ZZ $\geq V_{DD} - 0.2V$ /CE, /WE, /OE $\geq V_{DD} - 0.2V$ /LB, /UB $\geq V_{DD} - 0.2V$ Others $\geq V_{DD} - 0.2V$ or $\leq 0.2V$	—	30	150	μA
Sleep Current	I_{ZZ}	/ZZ = V_{SS} /CE, /WE, /OE $\geq V_{DD} - 0.2V$ /LB, /UB $\geq V_{DD} - 0.2V$ Others $\geq V_{DD} - 0.2V$ or $\leq 0.2V$	—	5	20	μA
High Level Output Voltage	V_{OH1}	$V_{DD} = 2.7V$ to $3.6V$ $I_{OH} = -1.0mA$	$V_{DD} \times 0.8$	—	—	V
	V_{OH2}	$V_{DD} = 1.8V$ to $2.7V$ $I_{OH} = -100\mu A$	$V_{DD} - 0.2$	—	—	
Low Level Output Voltage	V_{OL1}	$V_{DD} = 2.7V$ to $3.6V$ $I_{OL} = 2.0mA$	—	—	0.4	V
	V_{OL2}	$V_{DD} = 1.8V$ to $2.7V$ $I_{OL} = 150\mu A$	—	—	0.2	

*1: During the measurement of I_{DD} , all Address and I/O were taken to only change once per active cycle.
Iout : output current

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2. AC Characteristics

• AC Test Conditions

Power Supply Voltage	: 1.8 V to 3.6 V
Operation Ambient Temperature	: -40 °C to +85 °C
Input Voltage Amplitude	: 0 V / V_{DD}
Input Rising Time	: 3 ns
Input Falling Time	: 3 ns
Input Evaluation Level	: $V_{DD}/2$
Output Evaluation Level	: $V_{DD}/2$
Output Load Capacitance	: 30 pF

(1) Read Cycle

Parameter	Symbol	Value ($V_{DD}=1.8V$ to $2.7V$)		Value ($V_{DD}=2.7V$ to $3.6V$)		Unit
		Min	Max	Min	Max	
Read Cycle time	t_{RC}	185	—	150	—	ns
/CE Access Time	t_{CE}	—	95	—	75	ns
Address Access Time	t_{AA}	—	185	—	150	ns
/OE Output Data Hold time	t_{OH}	0	—	0	—	ns
Output Data Hold time	t_{OAH}	20	—	20	—	ns
/CE Active Time	t_{CA}	95	—	75	—	ns
Pre-charge Time	t_{PC}	90	—	75	—	ns
/LB, /UB Access Time	t_{BA}	—	35	—	20	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Address Hold Time	t_{AH}	95	—	75	—	ns
/OE Access Time	t_{OE}	—	35	—	20	ns
/CE Output Floating Time	t_{HZ}	—	10	—	10	ns
/OE Output Floating Time	t_{OHZ}	—	10	—	10	ns
/LB, /UB Output Floating Time	t_{BHZ}	—	10	—	10	ns
Address Transition Time	t_{AX}	—	10	—	10	ns

(2) Write Cycle

Parameter	Symbol	Value (V _{DD} =1.8V to 2.7V)		Value (V _{DD} =2.7V to 3.6V)		Unit
		Min	Max	Min	Max	
Write Cycle Time	t _{WC}	185	—	150	—	ns
/CE Active Time	t _{CA}	95	—	75	—	ns
/CE↓ to /WE↑ Time	t _{CW}	95	—	75	—	ns
Pre-charge Time	t _{PC}	90	—	75	—	ns
Write Pulse Width	t _{WP}	20	—	20	—	ns
Address Setup Time	t _{AS}	0	—	0	—	ns
Address Hold Time	t _{AH}	95	—	75	—	ns
/WE↓ to /CE↑ Time	t _{WLC}	30	—	25	—	ns
Address Transition to /WE↑ Time	t _{AWH}	185	—	150	—	ns
/WE↑ to Address Transition Time	t _{WHA}	0	—	0	—	ns
/LB, /UB Setup Time	t _{BS}	2	—	2	—	ns
/LB, /UB Hold Time	t _{BH}	0	—	0	—	ns
Data Setup Time	t _{DS}	20	—	20	—	ns
Data Hold Time	t _{DH}	0	—	0	—	ns
/WE Output Floating Time	t _{WZ}	—	10	—	10	ns
/WE Output Access Time ^{*1}	t _{WX}	10	—	10	—	ns
Write Setup Time ^{*1}	t _{WS}	0	—	0	—	ns
Write Hold Time ^{*1}	t _{WH}	0	—	0	—	ns

*1: Writing operation applies “Write Cycle Timing 1” or “Write Cycle Timing 2” by the relation of /CE and /WE timing. The values of t_{WX}, t_{WS} and t_{WH} are defined by these operations. The conditions of t_{WS} and t_{WH} are not checked at shipping test.

(3) Power ON/OFF Sequence and Sleep Mode Cycle

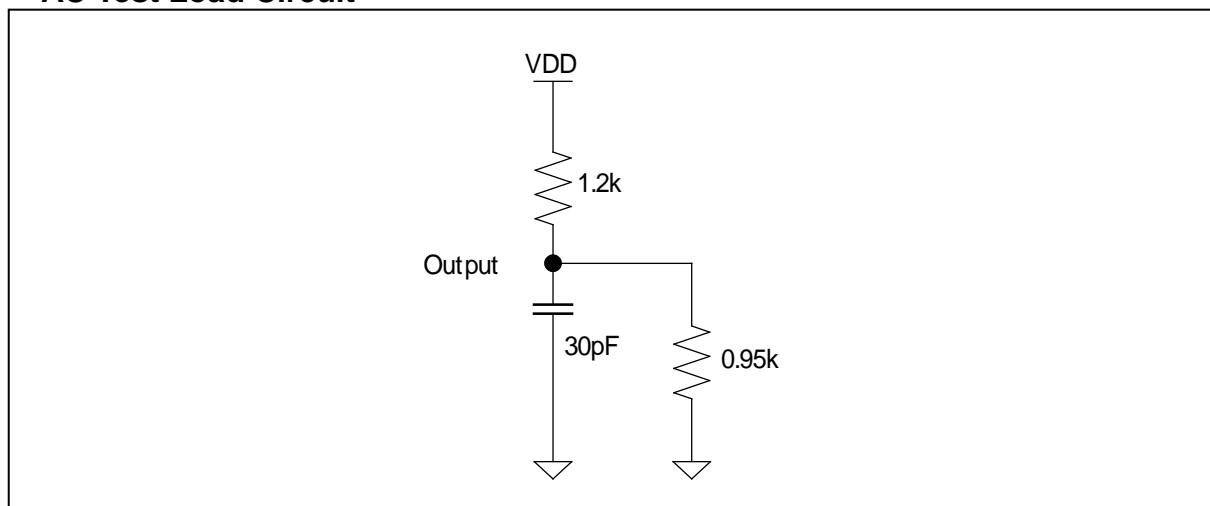
Parameter	Symbol	Value		Unit
		Min	Max	
/CE level hold time for Power ON	t _{PU}	450	—	μs
/CE level hold time for Power OFF	t _{PD}	85	—	ns
Power supply rising time	t _{VR}	50	—	μs/V
Power supply falling time	t _{VF}	100	—	μs/V
/ZZ active time	t _{ZZL}	1	—	μs
Sleep mode enable time	t _{ZZEN}	—	0	μs
Sleep mode release time	t _{ZZEX}	—	450	μs

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3. Pin Capacitance

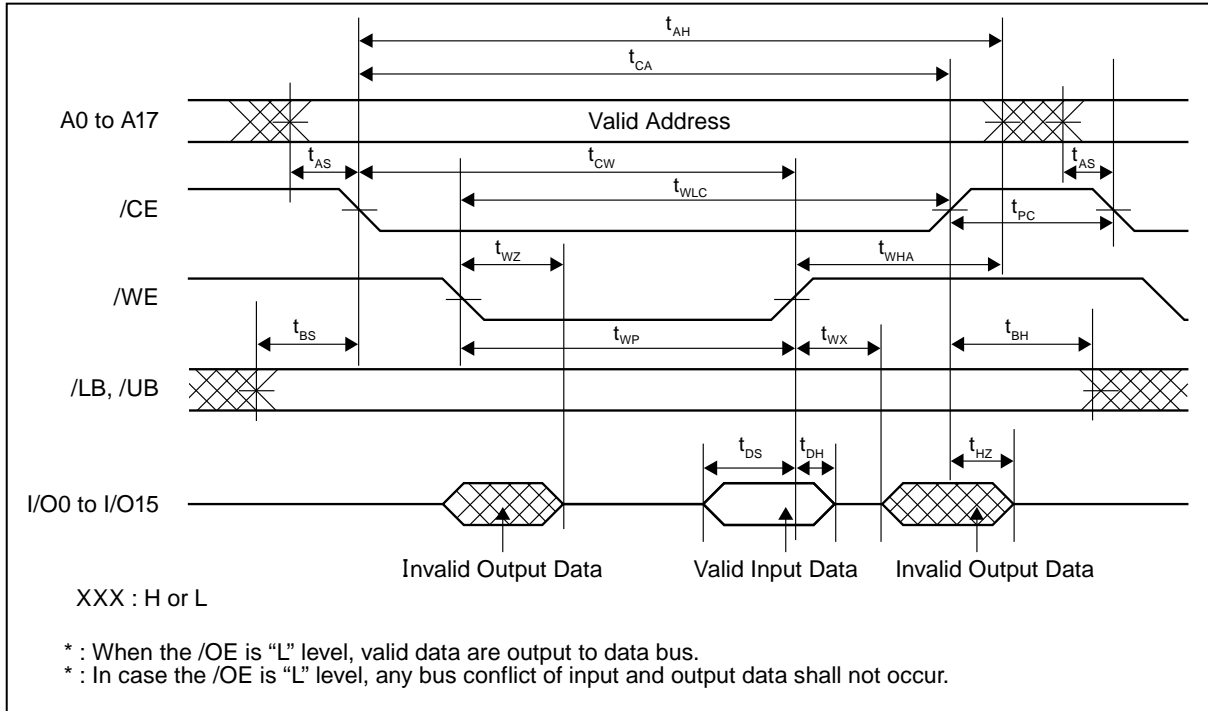
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Capacitance	C_{IN}	$V_{DD} = 3.3\text{ V}$, $f = 1\text{ MHz}$, $T_A = +25\text{ }^\circ\text{C}$	—	—	6	pF
Input/Output Capacitance (I/O pin)	C_{IO}		—	—	8	pF
/ZZ Pin Input Capacitance	C_{ZZ}		—	—	8	pF

■ AC Test Load Circuit

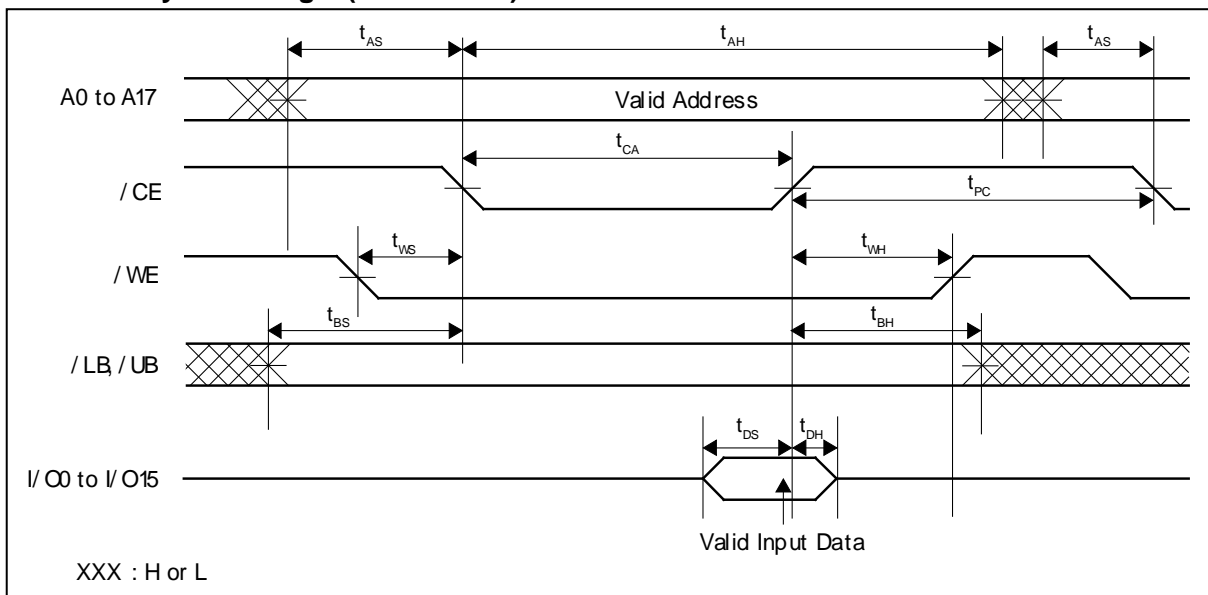


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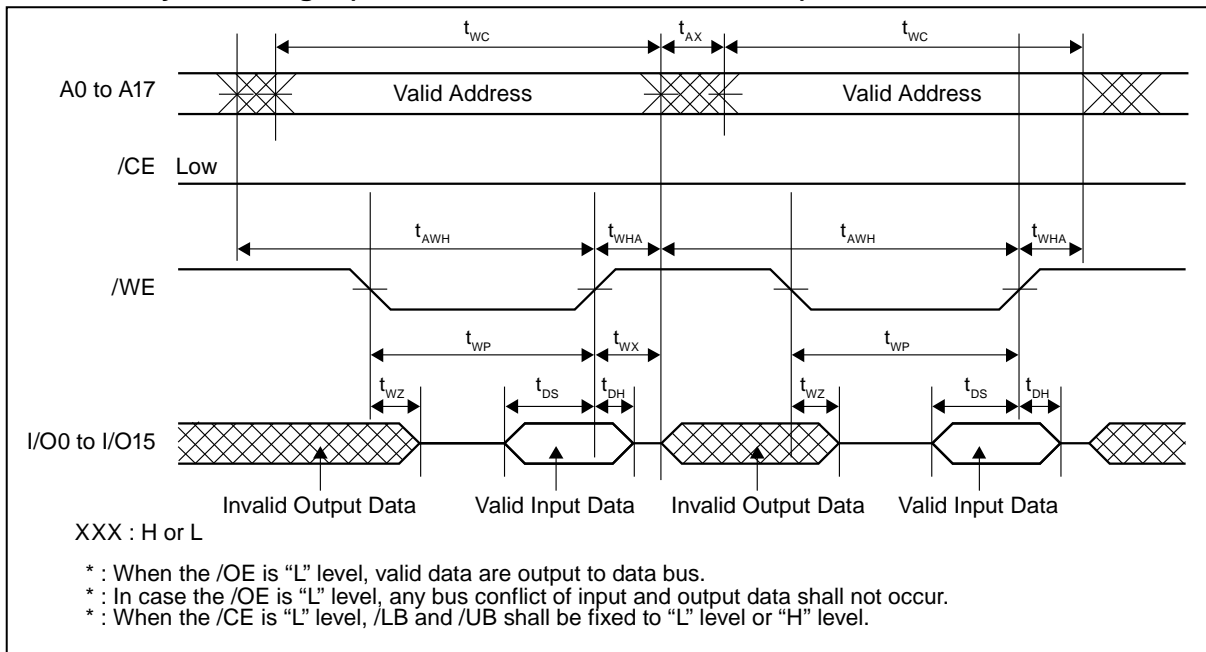
3. Write Cycle Timing 1 (/WE Control)



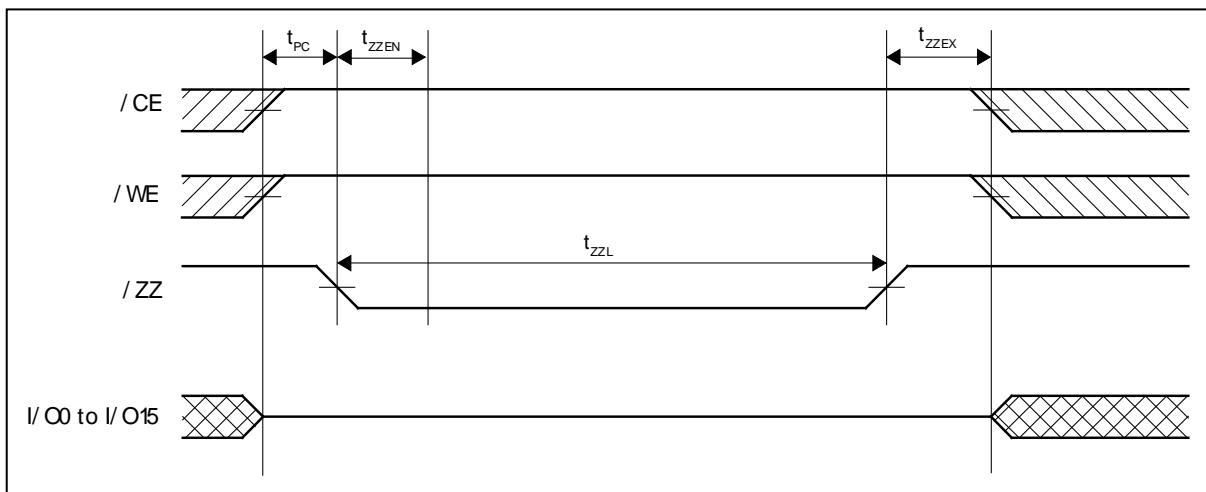
4. Write Cycle Timing 2 (/CE Control)



5. Write Cycle Timing 3 (Address Access and /WE Control)

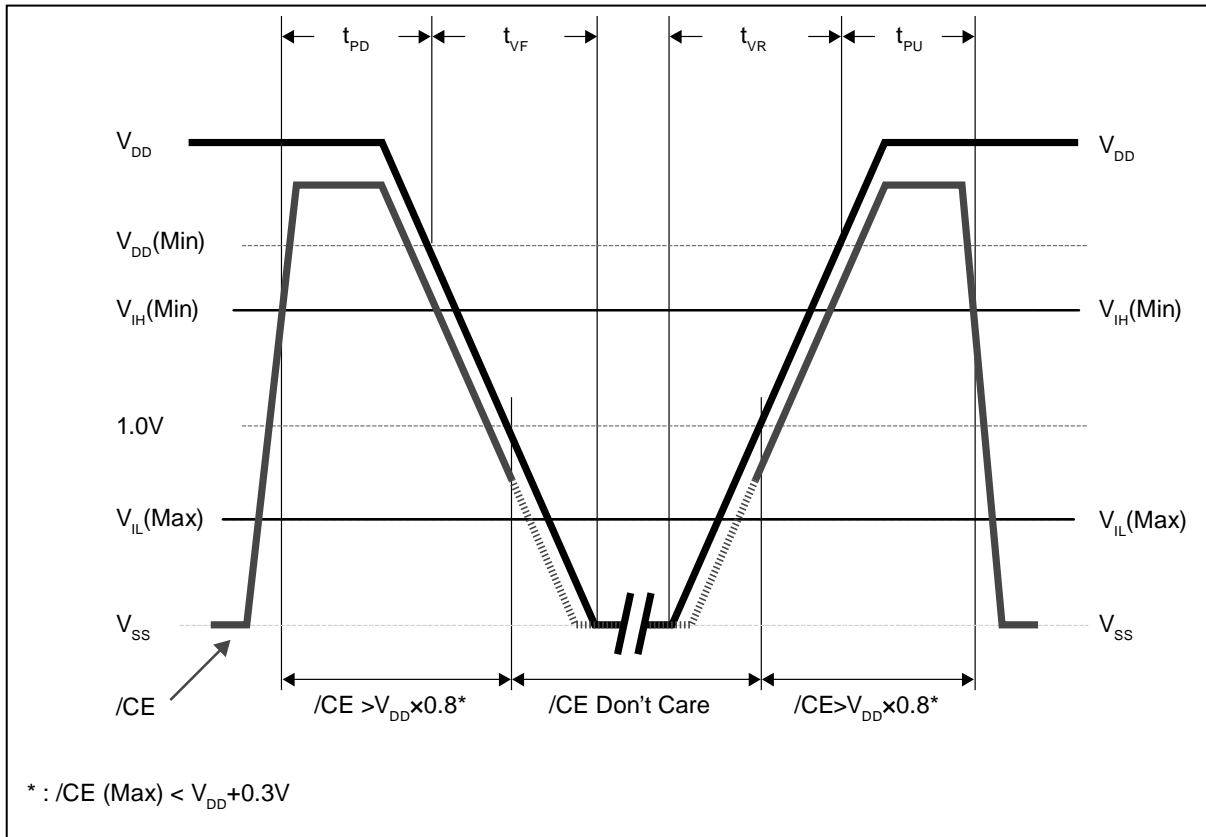


6. Sleep Mode Timing



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■ POWER ON/OFF SEQUENCE



■ FRAM CHARACTERISTICS

Item	Min	Max	Unit	Parameter
Read/Write Endurance ^{*1}	10^{13}	—	Times/16 bits	Operation Ambient Temperature $T_A = +85\text{ }^\circ\text{C}$
Data Retention ^{*2}	10	—	Years	Operation Ambient Temperature $T_A = +85\text{ }^\circ\text{C}$

*1: Total number of reading and writing defines the minimum value of endurance, as an FRAM memory operates with destructive readout mechanism.

*2: Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

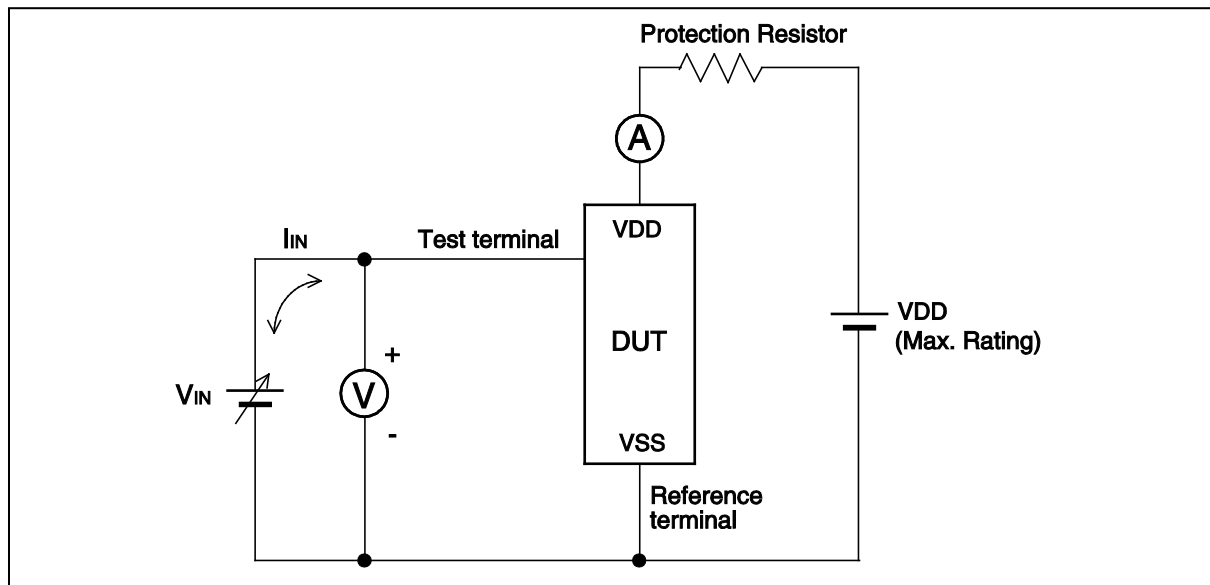
■ NOTE ON USE

- We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

■ ESD AND LATCH-UP

Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85R4M2TFN-G-ASE1	$\geq 2000 \text{ V} $
ESD MM (Machine Model) JESD22-A115 compliant		$\geq 200 \text{ V} $
ESD CDM (Charged Device Model) JESD22-C101 compliant		—
Latch-Up (I-test) JESD78 compliant		—
Latch-Up (V_{supply} overvoltage test) JESD78 compliant		—
Latch-Up (Current Method) Proprietary method		—
Latch-Up (C-V Method) Proprietary method		$\geq 200 \text{ V} $

▪ Current method of Latch-Up Resistance Test



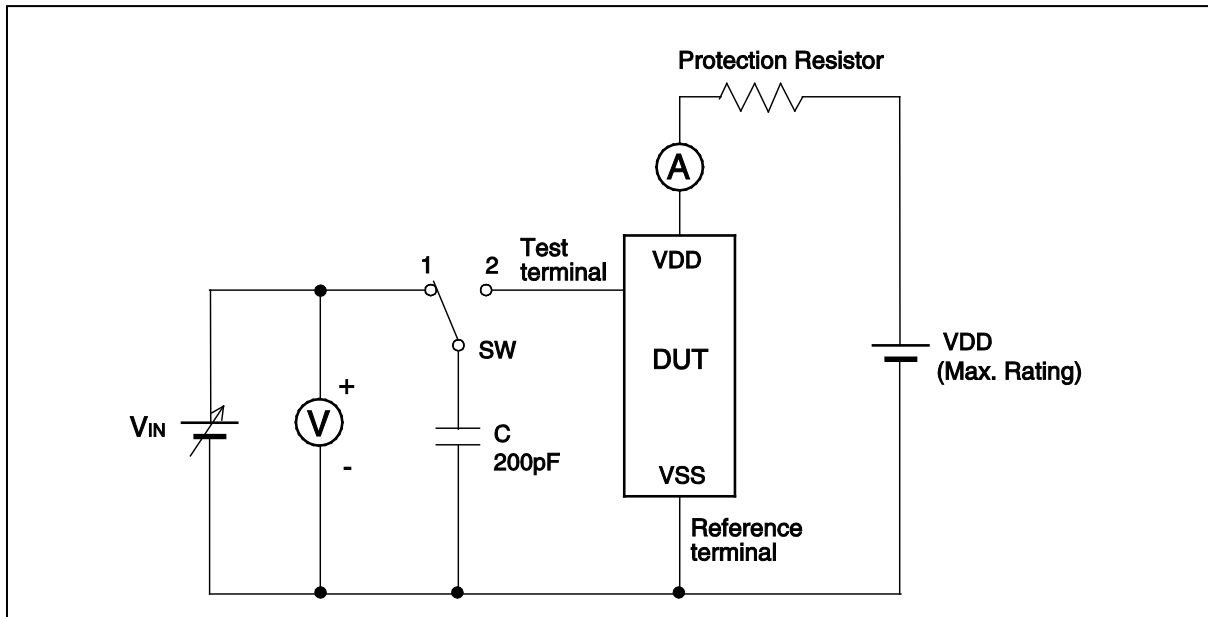
Note: The voltage V_{IN} is increased gradually and the current I_{IN} of 300 mA at maximum shall flow.

Confirm the latch up does not occur under $I_{IN} = \pm 300 \text{ mA}$.

In case the specific requirement is specified for I/O and I_{IN} cannot be 300 mA, the voltage shall be increased to the level that meets the specific requirement.

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▪ C-V method of Latch-Up Resistance Test



Note: Charge voltage alternately switching 1 and 2 approximately 2 sec intervals. This switching process is considered as one cycle.

Repeat this process 5 times. However, if the latch-up condition occurs before completing 5times, this test must be stopped immediately.

■ REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (ISP/JEDEC J-STD-020D)

■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS. Please refer to the following web site for more details of current status on contained restricted substances in our products.

<http://www.fujitsu.com/global/services/microelectronics/environment/products/>

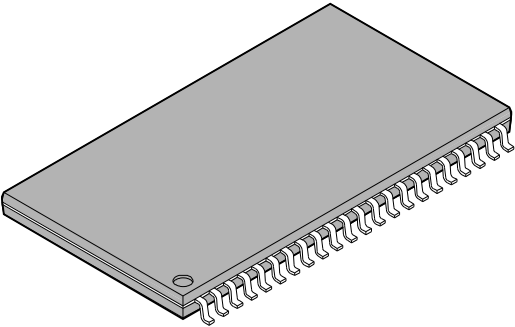
■ ORDERING INFORMATION

Part Number	Package	Shipping form	Minimum shipping quantity
MB85R4M2TFN-G-ASE1	44-pin plastic TSOP (FPT-44P-M34)	Tray	—*

*: Please contact our sales office about minimum shipping quantity.

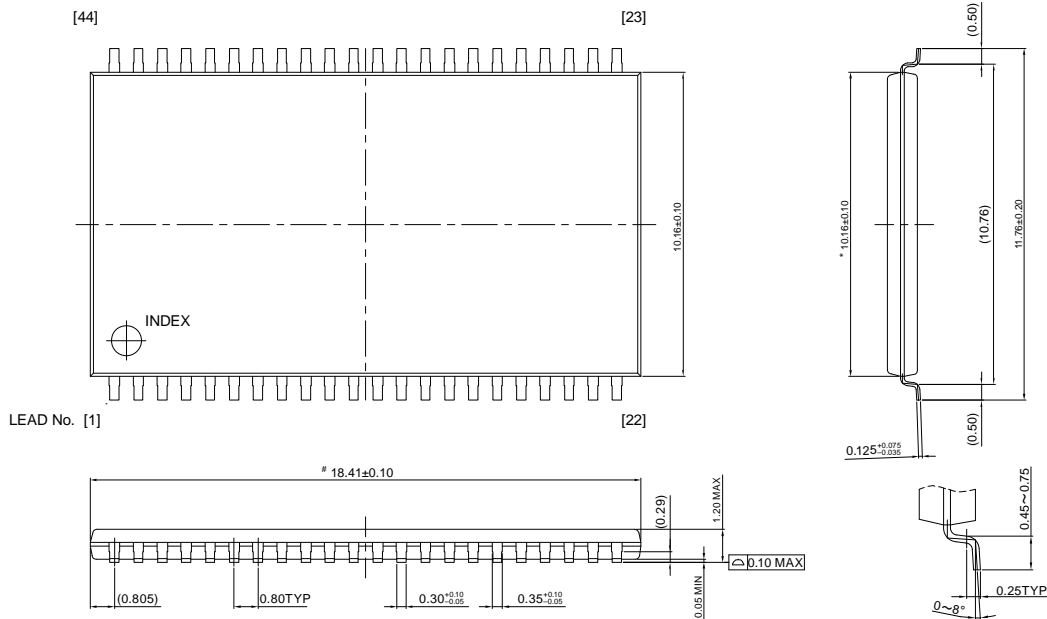
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■ PACKAGE DIMENSIONS

<p>44-pin plastic TSOP</p>  <p>(FPT-44P-M34)</p>	Lead pitch	0.8mm
	Package width × package length	10.16 × 18.41mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.2mm
	Weight	TBD

44-pin plastic TSOP
(FPT-44P-M34)

Note 1) # : Resin protrusion.(Each side:+0.15 Max).
 Note 2) * : These dimensions do not include resin protrusion.
 Note3) Pins width and pins thickness include plating thickness.
 Note4) Pins width do not include tie bar cutting remainder.

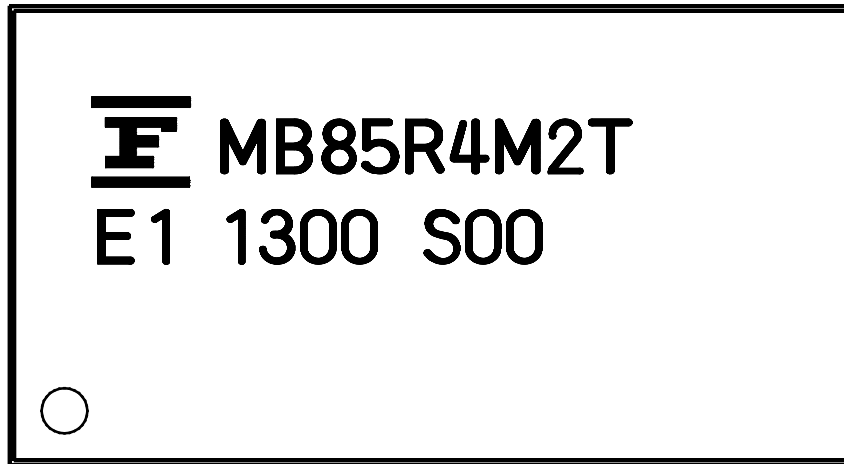


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Dimensions in mm.
 Note : The values in parentheses are reference values.

■ MARKING

[MB85R4M2TFN-G-ASE1]



[FPT-44P-M34]

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■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
6	■ RECOMMENDED OPERATING CONDITIONS	Revised the Low Level Input Voltage.
7 to 9	■ ELECTRICAL CHARACTERISTICS 1. DC Characteristics 2. AC Characteristics	Revised the TBD value. Delete the timing of /UB↓ or /LB↓ to /CE↑. Correct the unit of /ZZ active time.
12	3. Write Cycle Timing 1 (/WE Control)	Add note in case of /OE=L.
	4. Write Cycle Timing 2 (/CE Control)	Change timing of /LB and /LU.
13	5. Write Cycle Timing 3 (Address Access and /WE Control)	Add note in case of /OE=L and /CE=L.
14	■ FRAM CHARACTERISTICS	Add clause.
	■ NOTE ON USE	Delete the note about PON.
15,16	■ ESD AND LATCH-UP	Add clause.
16	■ REFLOW CONDITION AND FLOOR LIFE	Add clause.
	■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES	
19	■ MARKING	Add clause.

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