General Description

The MAX14720/MAX14750 are compact power-management solutions for space-constrained, battery-powered applications where size and efficiency are critical. Both devices integrate a power switch, a linear regulator, a buck regulator, and a buck-boost regulator.

The MAX14720 is designed to be the primary power-management device and is ideal for either non-rechargeable battery (coin-cell, dual alkaline) applications or for rechargeable solutions where the battery is removable and charged separately. The device includes a button monitor and sequencer.

The MAX14750 works well as a companion to a charger or PMIC in rechargeable applications. It provides direct pin control of each function and allows greater flexibility for controlling sequencing.

The devices include two programmable micro-I_Q, high-efficiency switching converters: a buck-boost regulator and a synchronous buck regulator. These regulators feature a burst mode for increased efficiency during light-load operation.

The low-dropout linear regulator has a programmable output. It can also operate as a power switch that can disconnect the quiescent load of system peripherals.

The devices also include a power switch with battery-monitoring capability. The switch can isolate the battery from all system loads to maximize battery life when not operating. It is also used to isolate the battery-impedance measurements. This switch can operate as a general-purpose load switch as well.

The MAX14720 includes a programmable power controller that allows the device to be configured either for use in applications that require a true off state or for always-on applications. This controller provides a delayed reset signal, voltage sequencing, and customized button timing for on/off control and recovery hard reset.

Both devices also include a multiplexer for monitoring the power inputs and outputs of each function.

These devices are available in a 25-bump, 0.4mm pitch, 2.26mm x 2.14mm wafer-level package (WLP) and operate over the -40°C to +85°C extended temperature range.

Benefits and Features

- Extended System Battery Use Time
  - Micro-I_Q 250mW Buck-Boost Regulator
    - Input Voltage from 1.8V to 5.5V
    - Output Voltage Programmable from 2.5V to 5V
    - 1.1µA Quiescent Current
    - Programmable Current Limit
  - Micro-I_Q 200mA Buck Regulator
    - Input Voltage from 1.8V to 5.5V
    - Output Voltage Programmable from 1.0V to 2.0V
    - 0.9µA Quiescent Current
  - Micro-I_Q 100mA LDO
    - Input Voltage From 1.71V to 5.5V
    - Output Programmable From 0.9V to 4.0V
    - 0. 9µA Quiescent Current
    - Configurable as Load Switch
- Extend Product Shelf-Life
  - Battery Seal Mode (MAX14720)
    - 120nA Battery Current
  - Power Switch On-Resistance
    - 250mΩ (max) at 2.7V
    - 500mΩ (max) at 1.8V
  - Battery Impedance Detector
- Easy-to-Implement System Control
  - Configurable Power Mode and Reset Behavior (MAX14720)
    - Push-Button Monitoring to Enable Ultra-Low Power Shipping Mode
    - Disconnects All Loads From Battery and Reduces Leakage to Less than 1µA
    - Power-On Reset (POR) Delay and Voltage Sequencing
  - Individual Enable Pins (MAX14750)
  - Voltage Monitor Multiplexer
  - I^2C Control Interface

Applications

- Wearable Medical Devices
- Wearable Fitness Devices
- Portable Medical Devices

***Ordering Information* appears at end of data sheet.**

Absolute Maximum Ratings

(Voltages Referenced to GND.)
BIN, LIN, SDA, SCL, SWIN, BEN, SWOUT, SWEN, LEN, HVEN, HVIN, HVOUT, MON, CAP, V_{CC}, MPC, $\overline{KIN}$, $\overline{RST}$, $\overline{KOUT}$ .... -0.3V to +6.0V
HVILX ....-0.3V to V_{HVIN} + 0.3V
HVOLX ....-0.3V to V_{HVOUT} + 0.3V
BLX, BOUT..-0.3V to (V_{BIN} + 0.3V)
LOUT .... -0.3V to (V_{LIN} + 0.3V)
GND...-0.3V to +0.3V
Continuous-Current into HVIN, BIN, SWIN ....±1000mA
Continuous-Current into Any Other Terminal ....±100mA
Continuous Power Dissipation (multilayer board at +70°C):
5x5 Array 25-Ball 2.26mm x 2.14mm 0.4mm Pitch WLP (derate 19.07mW/°C)..1.525W
Operating Temperature Range .... -40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering 10s) ....+300°C
Soldering Temperature (reflow).....................................+260°C

Package Thermal Characteristics (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....52.43°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = V_{BIN} = V_{LIN} = V_{HVIN} = V_{SWIN} = 2.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENT						
Seal Input Current	I_{SEAL}	Seal mode, all functions disabled		0.12	1	µA
Off Input Current	I_{OFF}	No blocks enabled, no battery measurement active		1.2	2.8	µA
MON Input Current	I_{MON}	No blocks enabled, no battery measurement active, MON enabled, MONCtr[2:0] = 000.		4	7.2	µA
Switch Input Current	I_{SW}	Switch enabled, I_{SWOUT} = 0A		1.2	2.8	µA
LDO Input Current	I_{LDO}	LDO enabled, I_{LOUT} = 0A		2.1	4.4	µA
		LDO enabled, LIN UVLO enabled, I_{LOUT} = 0A		2.4	4.8	
		LDO enabled, switch mode, I_{LOUT} = 0A		1.5	3.2	
Buck Input Current	I_{BUCK}	Buck enabled, I_{BOUT} = 0A		2	4.1	µA
		Buck enabled, BIN UVLO enabled, I_{BOUT} = 0A		2.2	4.5	
Buck-Boost Input Current	I_{BCKBST}	Buck-Boost enabled, I_{HVOUT} = 0A, V_{HVOUT} = 4V		2	4.7	µA
		Buck-Boost enabled, BIN UVLO enabled, I_{HVOUT} = 0A, V_{HVOUT} = 4V		2.3	5	

Electrical Characteristics (continued)

(V_{CC} = V_{BIN} = V_{LIN} = V_{HVIN} = V_{SWIN} = 2.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
On Input Current	I_{ON}	LDO, buck, and buck-boost enabled; BIN UVLO and LIN UVLO enabled; I_{SWOUT} = I_{LOUT} = I_{BOUT} = I_{HVOUT} = 0A		4.4	8.3	µA
POWER SEQUENCE						
Boot Time	t_{BOOT}	MAX14720	9.9	11	12.1	ms
		MAX14750	21.6	24	26.4	ms
Reset Time	t_{RST}	MAX14720	72	80	88	ms
POWER SWITCH						
Input Voltage Range	V_{SWIN}	$V_{SWIN} \leq V_{CC}$	1.8		5.5	V
Quiescent Supply Current	I_{Q_SW}	I_{SWOUT} = 0A		0.05	0.09	µA
Switch On-Resistance	R_{ON_SW}	I_{SWOUT} = 200mA		0.16	0.25	Ω
		V_{SWIN} = 1.8V, I_{SWOUT} = 200mA		0.27	0.5	
Maximum Output Current	I_{SWOUT_MAX}		200			mA
Turn-On Time	t_{ON_SW}	I_{SWOUT} = 0mA, C_{SWOUT} = 100µF, time from 10% to 90% of V_{SWIN}, SWSoftStart = 0		0.65		ms
		I_{SWOUT} = 0mA, C_{SWOUT} = 100µF, time from 10% to 90% of V_{SWIN}, SWSoftStart = 1		13.8		ms
Short-Circuit Current Limit	I_{SHRT_SW}	V_{SWOUT} = GND, SWSoftStart = 0	200	460	700	mA
Soft-Start Current Limit	I_{SSTR_SW}	V_{SWOUT} = GND, SWSoftStart = 1	9	25	54	mA
Thermal-Shutdown Threshold	T_{SHDN_SW}	T_J rising		150		°C
Thermal-Shutdown Hysteresis	$T_{SHDN\_HYST\_SW}$			20		°C
BUCK BOOST CONVERTER (C_{OUT} = 10MF, L = 4.7MF, unless otherwise noted.)						
Input Voltage Range	V_{HVIN}		1.8		5.5	V
Quiescent Supply Current	I_{Q_BOOST}	V_{HVOUT} = 4V, I_{HVOUT} = 0A, BIN UVLO disabled		1.1	2.6	µA
		V_{HVOUT} = 4V, I_{HVOUT} = 0A, BIN UVLO enabled		1.3	3	µA
Minimum Input Voltage Startup	V_{HVIN_STUP}	I_{LOAD} = 1mA, minimum input voltage for correct startup of the buck-boost	1.9			V

Electrical Characteristics (continued)

(V_{CC} = V_{BIN} = V_{LIN} = V_{HVIN} = V_{SWIN} = 2.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Output Operating Power	$P_{MAXHVOUT}$	V_{HVIN} = 3V	250			mW
Output Voltage	V_{HVOUT}	100mV step	2.5		5	V
Output Accuracy	ACC_{HVOUT}	I_{HVOUT} = 1mA, average output C_{OUT} ≥ 10µF	-3		+3	%
Line Regulation Error	$V_{HVINREG\_BOOST}$	V_{HVIN} = 1.8V to 5.5V, I_{HVOUT} = 10uA, V_{HVOUT} = 4V, I_{SET} = 100mA	-1	0.1	+1	%/V
Load Regulation Error	$V_{LOADREG\_BOOST}$	V_{HVOUT} = 4V, I_{HVOUT} = 10µA to 50mA, I_{SET} = 100mA		100		mV/A
		V_{HVOUT} = 4V, I_{HVOUT} = 10µA to 100mA, I_{SET} = 100mA		310		mV/A
Line Transient	$V_{LINETRAN\_BST}$	V_{HVOUT} = 4V, I_{SET} = 100mA, V_{HVIN} = V_{CC} = 2.5V to 5V, 0.2µs rise time		15		mV
Load Transient	$V_{LOADTRAN\_BST}$	I_{HVOUT} = 0mA to 10mA, 200ns rise time, V_{HVOUT} = 4V, I_{SET} = 100mA		9		mV
		I_{HVOUT} = 0mA to 100mA, 200ns rise time, V_{HVOUT} = 4V, I_{SET} = 100mA		31		mV
Oscillator Frequency	f_{OSC_BST}		1.78	2	2.25	MHz
Passive Discharge Pulldown Resistance	R_{PDL_BST}		5	10	16	kΩ
Active Discharge Current	I_{ACTDL_BST}	V_{HVIN} = 3V	6	19	38	mA
Turn-On Time	t_{ON_BOOST}	Time from enable to full current capability		100		ms
UVLO on HVOUT	V_{HVOUT_UVLO}	UVLO voltage on HVOUT rising	1.6	1.75	1.9	V
UVLO Threshold Hysteresis	V_{UVLO_HYS}			150		mV
Precharge Current	I_{PC_BOOST}	Precharge current. V_{HVIN} = 1.8V, V_{HVOUT} = 1.65V	4	6.5	9	mA
Startup Input Current	I_{INSTUP_BST}	Input startup current. V_{HVIN} = 1.8V, V_{HVOUT} = 1.6V		11		mA
Startup Output Current	I_{OSTUP_BST}	Output startup current. V_{HVIN} = 1.8V, V_{HVOUT} = 5V		6.5		mA
Pulse Mode Input Current Limit	I_{PLS_IN}	V_{HVOUT} = 4V, V_{HVIN} < V_{HVOUT} - 0.5V, f_{SW} = f_{OSC}/10, I_{SET} = 100mA		6.6		mA

Electrical Characteristics (continued)

(V_{CC} = V_{BIN} = V_{LIN} = V_{HVIN} = V_{SWIN} = 2.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pulse Mode Switching Period Ratio	T_{RATIO}	f_{OSC}/f_{SW}, 128 steps	10		138	
Short-Circuit Peak Current Limit	I_{SHRT_BOOST}	V_{HVOUT} = GND.	0.4	1.1	1.9	A
Thermal-Shutdown Threshold	T_{SHDN_BST}	T_J rising		150		°C
Thermal-Shutdown Hysteresis	$T_{SHDN\_HYST\_BST}$			21		°C
BUCK CONVERTER (C_{OUT} = 10MF, L = 2.2MH, unless otherwise noted.)						
Input Voltage Range	V_{BIN}		1.8		5.5	V
Quiescent Supply Current	I_{Q_BUCK}	I_{BOUT} = 0A		0.8	1.6	µA
		I_{BOUT} = 0A, BIN UVLO enabled		1	2	µA
		I_{BOUT} = 0A, BuckMd[1:0] = 01			4.8	mA
Maximum Operative Output Current	$I_{MAXBOUT}$		250			mA
Output Voltage	V_{BOUT}	25mV step	1		2	V
Output Accuracy	A_{CC_BOUT}	V_{BIN} = (V_{BOUT} + 0.1V) or higher, I_{BOUT} = 1mA; average output	-3		+3	%
Dropout Voltage	V_{DROP_BUCK}	I_{BOUT} = 0A		95	120	mV
Line Regulation Error	$V_{LINEREG\_BUCK}$	V_{BIN} = from 2V to 5V, V_{BOUT} = 1.2V		0.65		%/V
Load Regulation Error	$V_{LOADREG\_BUCK}$	BuckInteg = 1, I_{BOUT} = 200mA		23		mV
Line Transient	$V_{LINETRAN\_BUCK}$	V_{BOUT} = 1.2V, V_{BIN} = V_{CC}: 2.0V to 5V, 1µs rise time		50		mV
Load Transient	$V_{LOADTRAN\_BUCK}$	I_{BOUT} = 0mA to 200mA, 200ns rise time		70		mV
Oscillator Frequency	f_{OSC_BK}		1.78	2	2.25	MHz
Passive Discharge Pull-Down Resistance	R_{PDL_BK}		5	10	16	kΩ
Active Discharge Current	I_{ACTDL_BK}		5.5	17	33	mA
Turn-On Time	t_{ON_BUCK}	Time from enable to full current capability; BuckFst = 0		60		ms
		Time from enable to full current capability; BuckFst = 1		30		ms
Startup Output Current	I_{STUP_BK}	BuckFst = 0		18		mA

Electrical Characteristics (continued)

(V_{CC} = V_{BIN} = V_{LIN} = V_{HVIN} = V_{SWIN} = 2.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Startup Output Current	I_{STUP_BK}	BuckFst = 1		42		mA
Short-Circuit Peak Current Limit	I_{SHRT_BUCK}	V_{BOUT} = GND.	0.54	0.8	2.19	A
Thermal-Shutdown Threshold	T_{SHDN_BUCK}	T_J rising		150		°C
Thermal-Shutdown Hysteresis	$T_{SHDN\_HYST\_BUCK}$			21		°C
LDO (C_{LOUT} = 1µF, unless otherwise noted. Typical values are with I_{LOUT} = 10mA, V_{LOUT} = 2V)						
Input Voltage Range	V_{LIN}	LDO mode	1.71		5.5	V
		Switch mode	1.2		5.5	
Quiescent Supply Current	I_{Q_LDO}	I_{LOUT} = 0A		0.9	1.9	µA
		I_{LOUT} = 0A, LIN UVLO enabled		1.1	2.2	
		I_{LOUT} = 0A, switch mode		0.3	0.5	
Quiescent Supply Current in dropout	$I_{Q\_LDO\_DRP}$	I_{LOUT} = 0A, V_{SET} = 2.8V		2.1	4.6	µA
Maximum Output Current	I_{LOUT_MAX}	V_{LIN} > 1.8V	100			mA
		V_{LIN} = 1.8V or lower	50			mA
Output Voltage	V_{LOUT}	100mV step	0.9		4	V
Output Accuracy	ACC_{LDO}	V_{LIN} = (V_{LOUT} + 0.5V) or higher, I_{LOUT} = 1mA	-3.1		+3.1	%
Dropout Voltage	V_{DROP_LDO}	V_{LIN} = V_{SET} = 2.7V, I_{LOUT} = 100mA			100	mV
Line Regulation Error	$V_{LINEREG\_LDO}$	V_{LIN} = (V_{LOUT} + 0.5 V) to 5.5V	-0.5		+0.5	%/V
Load Regulation Error	$V_{LOADREG\_LDO}$	V_{LIN} = 1.8V or higher, I_{LOUT} = 100µA to 100mA		0.001	0.005	%/mA
Line Transient	$V_{LINETRAN\_LDO}$	V_{LIN} = 4V to 5V, 200ns rise time		±35		mV
		V_{LIN} = 4V to 5V,1µs rise time		±25		mV
Load Transient	$V_{LOADTRAN\_LDO}$	I_{LOUT} = 0mA to 10mA, 200ns rise time		100		mV
		I_{LOUT} = 0mA to 100mA, 200ns rise time		200		mV
Passive Discharge Pulldown Resistance	R_{PDL_LDO}		4	10	18	kΩ
Active Discharge Current	I_{ACTDL_LDO}		5	20	40	mA

Electrical Characteristics (continued)

(V_{CC} = V_{BIN} = V_{LIN} = V_{HVIN} = V_{SWIN} = 2.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switch Mode Resistance	R_{ON_LDO}	V_{LIN} = 1.8V, I_{LOUT} = 50mA			1	Ω
		V_{LIN} = 1.2V, I_{LOUT} = 5mA			3	
Turn-On Time	t_{ON_LDO}	I_{LOUT} = 0mA , time from 10% to 90% of final regulation value		0.95		ms
		I_{LOUT} = 0mA , time from 10% to 90% of V_{LIN}, Switch mode		1.8		ms
Short-Circuit Current Limit	I_{SHRT_LDO}	V_{LOUT} = GND		380		mA
		V_{LOUT} = GND, Switch mode		370		mA
Thermal-Shutdown Threshold	t_{SHDN_LDO}	T_J rising		150		°C
Thermal-Shutdown Hysteresis	$t_{SHDN\_HYST\_LDO}$			21		°C
Output Noise	OUT_{NOISE_LDO}	10Hz to 100kHz, V_{LIN} = 5V, V_{LOUT} = 3.3V		150		μV_{RMS}
		10Hz to 100kHz, V_{LIN} = 5V, V_{LOUT} = 2.5V		125		
		10Hz to 100kHz, V_{LIN} = 5V, V_{LOUT} = 1.2V		90		
		10Hz to 100kHz, V_{LIN} = 5V, V_{LOUT} = 0.9V		80		
BATTERY IMPEDANCE MEASUREMENT						
SWOUT Allowed Supply Range	V_{SWOUT}		2		5.5	V
SWOUT UVLO	$U_{VLOSWOUT}$	Falling edge	1.92		2	V
SWOUT UVLO Hysteresis	$U_{VLOHYST}$	Hysteresis		30		mV
V_{CC} Impedance Test Current Range	I_{BIM_CUR}	Programmable current source with step change of 2x	250		8000	μA
V_{CC} Impedance Test Current Accuracy	I_{BIM_ACC}	V_{CC} > 1.2V	-10		10	%
V_{CC} Input Divider Resistance	R_{VCC}	V_{CC} measure enabled		1.5		MΩ
Measurable V_{CC} Voltage Range	V_{CC_FS}	Allowed V_{CC} voltages range for SAR ADC operation	1.2		3.6	V
V_{CC} Voltage Resolution LSB	V_{CC_LSB}			10.2		mV

Electrical Characteristics (continued)

(V_{CC} = V_{BIN} = V_{LIN} = V_{HVIN} = V_{SWIN} = 2.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Worst-Case Accuracy of Single V_{CC} Measurement	V_{CC_ACC}	V_{CC} = 1.2V	-72		+72	mV
		V_{CC} = 3.6V	-100		+100	
Worst-Case Accuracy Of Differential V_{CC} Measurement	$V_{CC\_ACC\_DIFF}$	$V_{CC1} - V_{CC2}$ = 100mV	-22		+22	%
		$V_{CC1} - V_{CC2}$ = 1.0V	-3.5		+3.5	
V_{CC} Voltage Wait Time Accuracy	t_{WAIT_ACC}	10ms, 100ms, 1s programmable t_{WAIT}	-10		+10	%
SAR ADC V_{CC} Voltage Conversion Time	t_{CONV}	Actual full V_{CC} measurement time is t_{WAIT} + t_{CONV}		120		µs
MONITOR MULTIPLEXER						
SWIN To MON Switch Resistance	R_{MON_SWIN}	V_{SWIN} > 1.8V, I_{LOAD} = 2mA		80	120	Ω
SWOUT/BIN/HVIN/ HVOUT/LIN To MON Switch Resistance	R_{MON_HV}	Sensed pin voltage > 1.8V, I_{LOAD} = 500µA			400	Ω
LOUT/BOUT To MON Switch Resistance	R_{MON_LV}	Sensed pin voltage > 0.9V, I_{LOAD} = 500µA			500	Ω
BBM Time	t_{BBM}	Anytime MONCtr[2:0] changed		80		µs
Pulldown Resistance	R_{MON_PD}	MONHiZ = 0		100		kΩ
UVLO/POR						
Input Voltage Range	V_{VCC}		1.8		5.5	V
BIN UVLO Threshold Rising	$V_{TH\_BIN\_RISE}$		1.68	1.73	1.77	V
BIN UVLO Threshold Falling	$V_{TH\_BIN\_FALLING}$		1.66	1.71	1.75	V
LIN UVLO Threshold Rising	$V_{TH\_LIN\_RISE}$		1.64	1.68	1.72	V
LIN UVLO Threshold Falling	$V_{TH\_LIN\_FALLING}$		1.62	1.66	1.7	V
POR Falling	$V_{TH\_POR\_FALLING}$	Seal mode	0.76	1.21		V
		No seal mode	1.55	1.66	1.77	V
POR Rising	$V_{TH\_POR\_RISING}$	Seal mode		1.27	1.71	V
		No seal mode	1.58	1.69	1.8	V

Electrical Characteristics (continued)

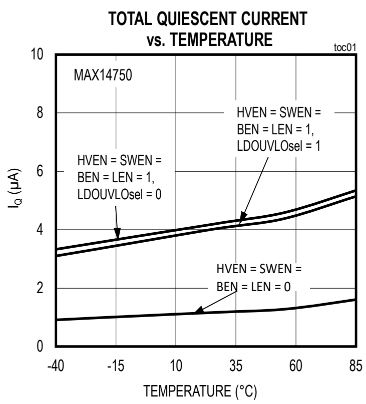
(V_{CC} = V_{BIN} = V_{LIN} = V_{HVIN} = V_{SWIN} = 2.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

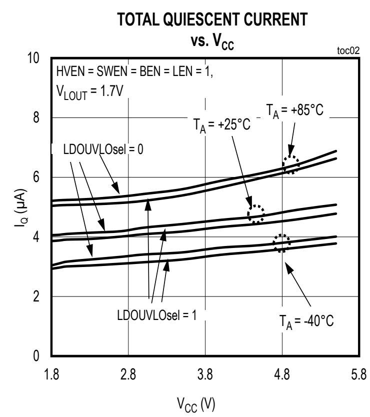
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL SIGNALS (V_{CC} = 1.8V to 5.5V, unless otherwise noted. Typical values are at V_{CC} = 2.7V.)						
Input Logic-High (SDA, SCL,SWEN,$\overline{KIN}$, BEN,MPC,LEN,HVEN)	V_{IH}	No seal mode	1.4			V
Input Logic-Low (SDA, SCL,SWEN,$\overline{KIN}$, BEN,MP,LEN,HVEN)	V_{IL}	No seal mode			0.45	V
		No seal mode, V_{CC} ≥ 2.7V			0.5	V
Input Logic-High, Seal Mode (SDA, SCL, $\overline{KIN}$, MPC)	V_{IH_SEAL}	Seal mode	4.1			V
		Seal mode, V_{CC} ≥ 2.7V	2.2			V
Input Logic-Low, Seal Mode (SDA, SCL, $\overline{KIN}$, MPC)	V_{IL_SEAL}	Seal mode			0.5	V
Output Logic-Low (SDA, $\overline{RST}$, $\overline{KOUT}$)	V_{OL}	I_{OL} = 4mA			0.4	V
SCL Clock Frequency	f_{SCL}		0		400	kHz
KIN Pullup Resistance	R_{KIN}			210		kΩ
Bus Free Time Between a Stop and Start Condition	t_{BUF}		1.3			µs
Start Condition (Repeated) Hold Time	$t_{HD:STA}$	(Note 3)	0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated Start Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Note 4)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Setup Time for Stop Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}		50			ns

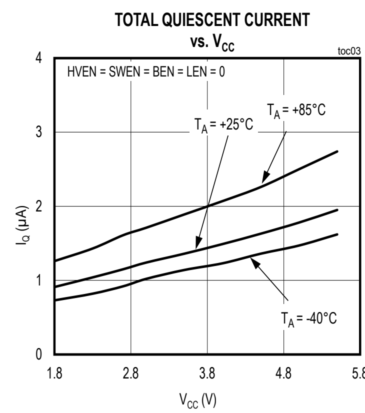
Note 2: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
Note 3: f_{SCL} must meet the minimum clock low time plus the rise/fall times.
Note 4: The maximum $t_{HD:DAT}$ has to be met only if the device does not stretch the low period (t_{LOW}) of the SCL signal.

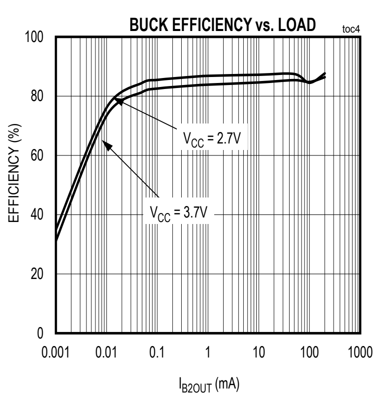
Typical Operating Characteristics

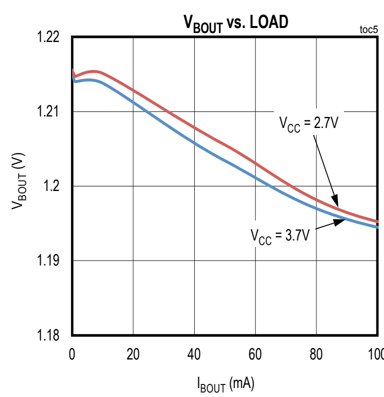
($V_{CC} = V_{BIN} = V_{LIN} = V_{HVIN} = V_{SWIN}$ = 2.7V, T_A = +25°C, all registers in their default state, unless otherwise noted.)

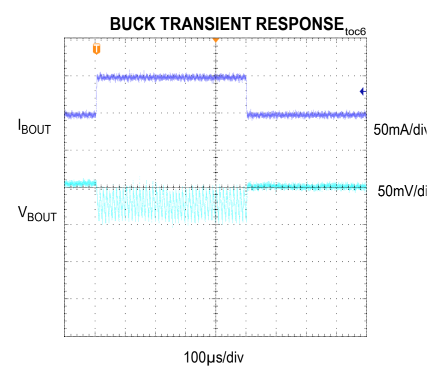


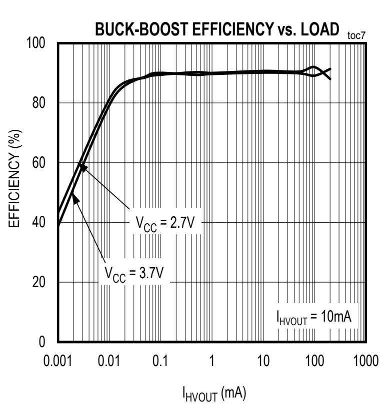


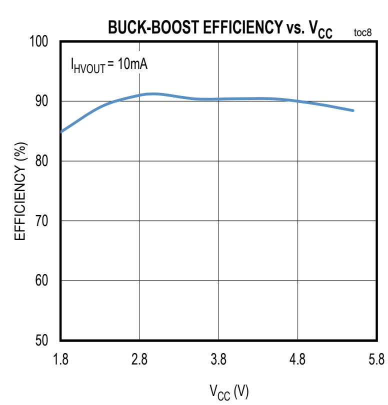


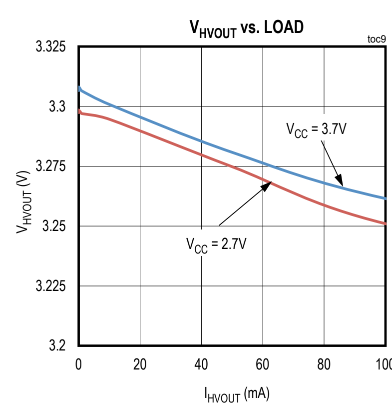






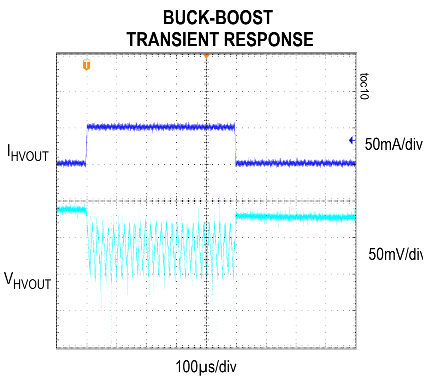


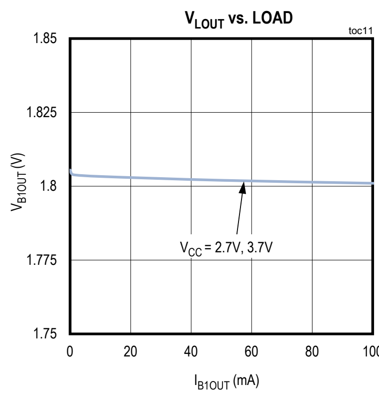


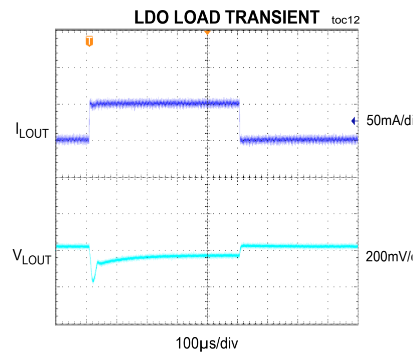


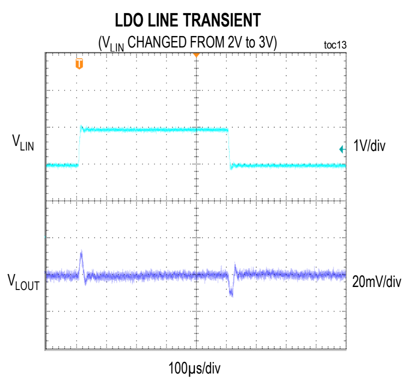
Typical Operating Characteristics (continued)

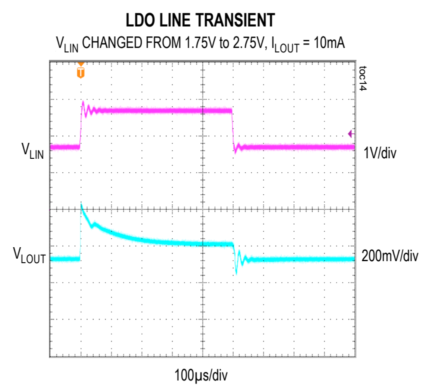
($V_{CC} = V_{BIN} = V_{LIN} = V_{HVIN} = V_{SWIN} = 2.7V$, $T_A = +25°C$, all registers in their default state, unless otherwise noted.)

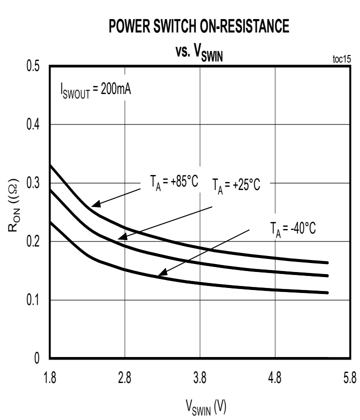


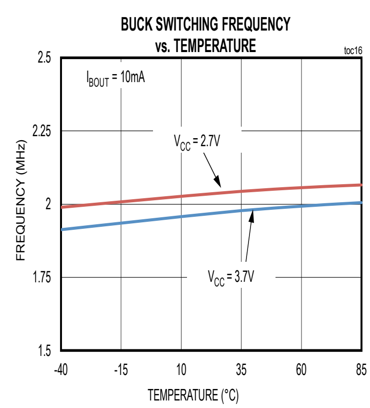




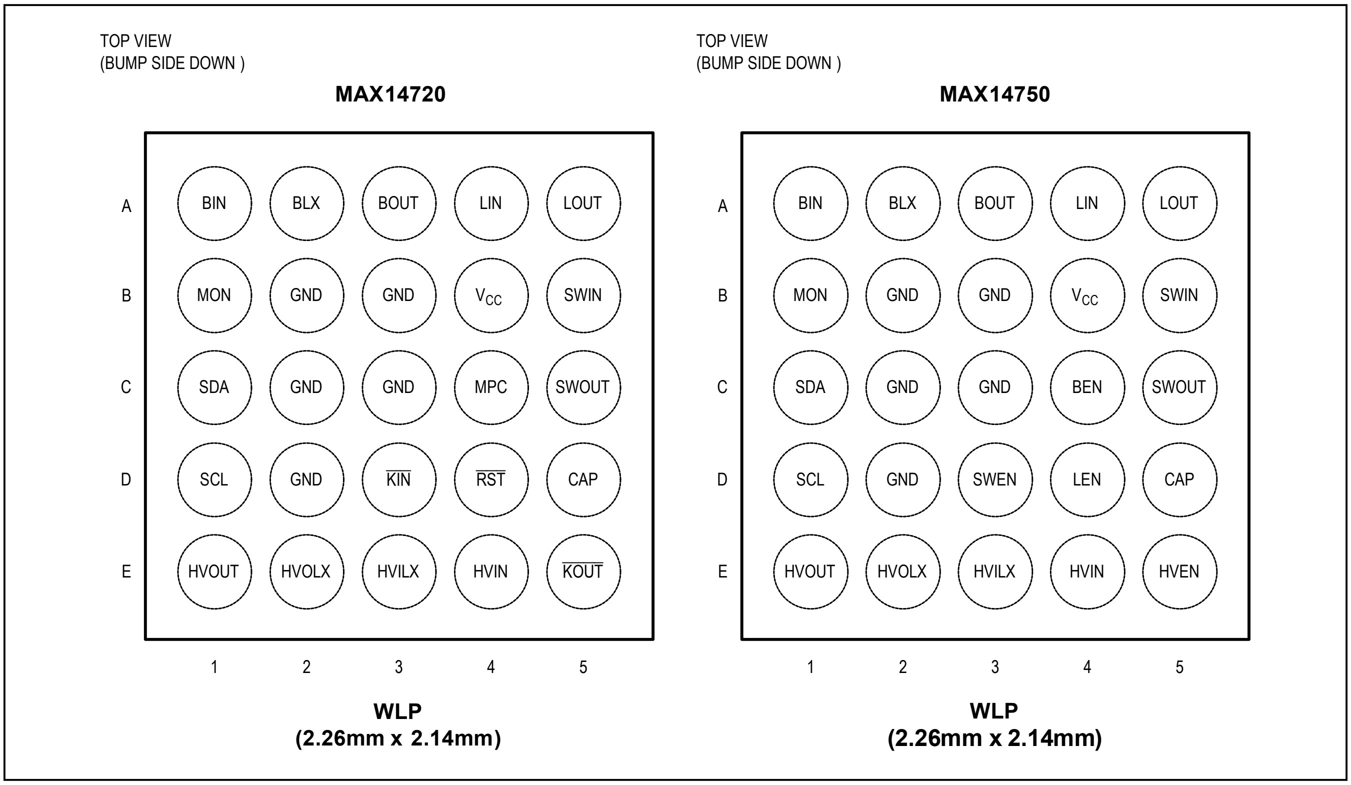








Bump Configurations



Bump Description

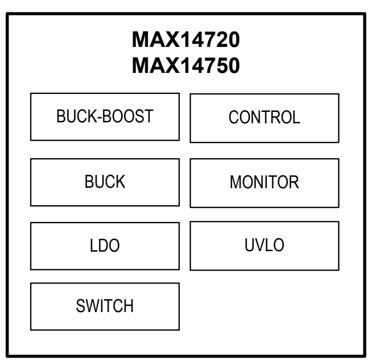
BUMP		NAME	FUNCTION
MAX14720	MAX14750		
A1	A1	BIN	Buck Regulator Input (must be connected to HVIN on the board). Bypass with a 1µF capacitor to GND.
A2	A2	BLX	Buck Regulator Switch
A3	A3	BOUT	Buck Regulator Output. Bypass with a 10µF capacitor to GND.
A4	A4	LIN	LDO Input. Bypass with a 1µF capacitor to GND.
A5	A5	LOUT	LDO Output. Bypass with a 1µF capacitor to GND.
B1	B1	MON	Monitor Multiplexer Output
B2, B3, C2, C3, D2	B2, B3, C2, C3, D2	GND	Ground
B4	B4	V_{CC}	Power Supply Input
B5	B5	SWIN	Power Switch Input. SWIN ≤ V_{CC}
C1	C1	SDA	Open-Drain I^2C Serial Data Input/Output
C4	—	MPC	Multipurpose Control Input
—	C4	BEN	Active-High Buck Regulator Enable Input

Bump Description (continued)

BUMP		NAME	FUNCTION
MAX14720	MAX14750		
C5	C5	SWOUT	Power Switch Output. Bypass with a 100μF capacitor to GND for battery impedance measurement.
D1	D1	SCL	I^2C Serial Clock
D3	—	$\overline{KIN}$	KEY Input. Active-low button monitor with internal 210kΩ pullup.
—	D3	SWEN	Active-High Power Switch Enable Input
D4	—	$\overline{RST}$	Active-Low, Open-Drain Reset Output
—	D4	LEN	Active-High Linear Regulator Enable Input
D5	D5	CAP	Internal Power Decoupling. Bypass with a 0.1μF capacitor to GND.
E1	E1	HVOUT	Buck-Boost Regulator Output. Bypass with a 10μF capacitor to GND.
E2	E2	HVOLX	Buck-Boost Regulator Boost Switch
E3	E3	HVILX	Buck-Boost Regulator Buck Switch
E4	E4	HVIN	Buck-Boost Regulator Input (Must be Connected to BIN on the Board). Bypass with a 1μF capacitor to GND.
E5	—	$\overline{KOUT}$	KEY Output. Active-low, open-drain buffered copy of $\overline{KIN}$.
—	E5	HVEN	Active-High Buck-Boost Regulator Enable Input

***Note:** All capacitance values listed in this document refer to effective capacitance. Be sure to specify capacitors that will meet these requirements under typical system operating conditions taking into consideration the effects of voltage and temperature.*

Block Diagram



Detailed Description

Power Regulation

The MAX14720/MAX14750 include a buck-boost regulator, a synchronous buck regulator, a low quiescent current linear regulator, and a power switch with integrated battery monitoring. Burst mode operation of the switching regulators provides excellent light-load efficiency and allows the switching regulators to run continuously without significant energy cost.

The buck-boost regulator in the devices is suitable for applications (such as low-power display biasing) that need the voltage present continuously while running from a battery. The buck-boost regulator can also operate in a current-limited mode to reduce current surges to the supply. The current-limiting is implemented by dividing down the frequency of the switching and is dependent on the ratio of the input-to-output voltage. Step-down operation is not allowed when current-limiting is active.

UVLO

In addition to the internal power-on-reset (POR) circuit, the devices also have two UVLO circuits that monitor the voltages on BIN and LIN pin to ensure that input voltages are sufficient for proper operation. It is required that the boost and buck-boost are powered from the same voltage so they share a UVLO on the BIN pin. The LDO has its own UVLO on the LIN pin. The UVLO circuits are disabled when the blocks are not enabled to reduce the quiescent current. The devices provide the ability to select which of the two UVLOs are used so that applications with BIN and LIN tied to the same supply can share a single UVLO to reduce quiescent current. The selection is made in the UVLOCfg register and the effects of the different settings are shown in the Table 1.

In the MAX14720, if there is a fault in a block that is enabled by the sequencer (every _Seq[2:0] option except 000, 110 or 111) the part will transition to the shutdown and then the off state. The part will remain off until the next button press. After the button press it will wait for the fault to clear before beginning the power on sequence. A fault is any condition that causes the block to turn off when it should be enabled, such as a UVLO condition or thermal shutdown.

Output Discharge

The regulators include circuitry to discharge their outputs. Active discharge applies a current sink, while passive discharge applies a load resistor. The active discharge is enabled during hard reset, or for 10ms as the part enters the off/seal mode. It can also be activated in the on state by a register bit when the regulator is disabled. Passive discharge is applied in the off/seal mode if the GlbPasDsc bit is set and can also be applied in the on state by a register bit when the regulator is disabled.

Power On/Off and Reset Control

The MAX14750 provides individual enable pins for each of the primary functions, while the MAX14720 includes a push-button monitor and sequencing controller. Figure 1 shows the basic flow diagram for the power-management control inside the MAX14720. Each primary function of the MAX14720 can be automatically enabled by the sequencing controller. The functions can default to be controlled by the I^2C configuration registers. The default state is determined by the factory configuration. See I^2C Register Descriptions section for more information.

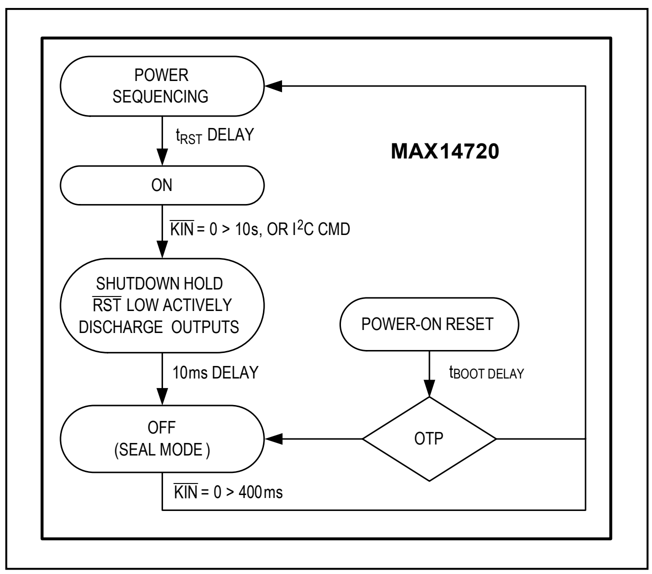


Figure 1. Power State Diagram for MAX14720

Table 1. UVLO Configuration

UVLOCfg	BBBUVLOsel	LDOUVLOsel	BIN UVLO	LIN UVLO
0x00	LIN	LIN	Disabled	Enabled
0x01	LIN	BIN	Enabled	Enabled
0x02	BIN	LIN	Enabled	Enabled
0x03	BIN	BIN	Enabled	Disabled

When the device begins the shutdown process, reset is driven low, all functions are disabled and outputs are actively discharged. Then, 10ms later, the device will be in the off state (seal mode) where all functions are disabled except for the power button monitor.

Power Sequencing (MAX14720 Only)

The sequencing of the voltage regulators during power-on is configurable. Each regulator can be configured to be turned on at one of four points during the power-on process. The four points are: t_{BOOT} after the power-on event, after the $\overline{RST}$ signal is released, or at two points in between. The two points in between are fixed proportionally to the duration of the POR process, but the overall time of the reset delay is configurable at 80ms, 120ms, 220ms, and 420ms. (Note that the actual turn-on time of some converters may be limited by the soft-starting of the output.) Figure 2 shows the timing relationship. Additionally, the regulators can be preselected to default off and can be turned on with an I²C command after reset is released.

Battery Impedance Measurement

The MAX14720 contains circuitry to measure the impedance of the power supply. To perform this measurement, SWIN must be connected to V_{CC}, with no capacitor present on the battery-side; all loads draw their power from the power-switch output (see *Typical Application Circuits*).

By default, the power switch is configured with a soft-start current limit that prevents potential high current drawn from the battery. This soft-start lasts 60ms after the power switch is turned on.

During battery measurement, the impedance measurement circuitry will open the power switch and record the voltage at the input to the switch before and after a current load is applied. During the measurement, the system must rely on the energy stored in the capacitor attached to the output of the switch for operation. If the SWOUT voltage falls below SWOUT UVLO threshold, the battery measurement is immediately aborted and the power switch closes.

The parameters of the current load and the timing of the pulse are specified in registers BatTime(0x0D) and BatCfg(0x0E) when the measurement is requested and the results are presented in registers BatV(0x0F), BatOCV(0x10), and BatLCV(0x11) (see Figure 3).

I²C Interface

The devices use the two-wire I²C interface to communicate with the host microcontroller. The configuration settings and status information provided through this interface are detailed in the register descriptions.

I²C Addresses

The registers of the devices are accessed through the slave address of 010101Ax (A is configurable by OTP).

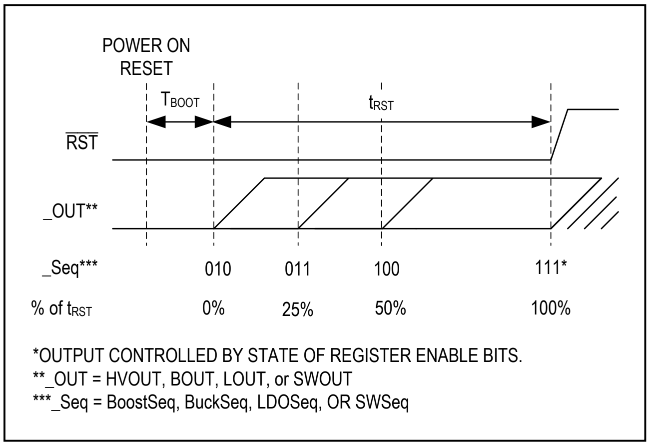


Figure 2. Reset Sequence Programming (MAX14720)

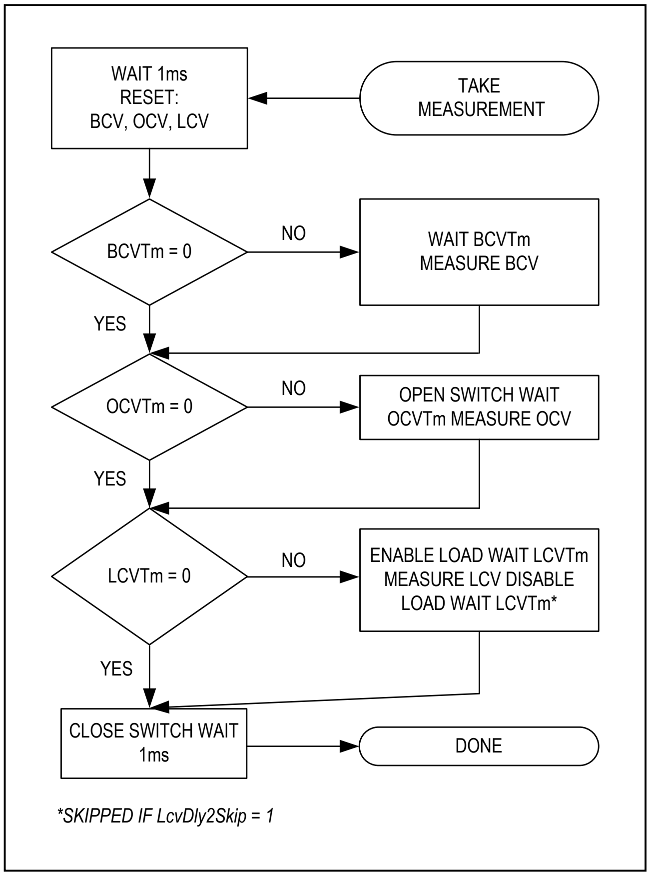


Figure 3. Battery Impedance Measurement

I²C Register Map

REGISTER ADDRESS	REGISTER NAME	B7	B6	B5	B4	B3	B2	B1	B0
0x00	ChipId	ChipId[7:0]*							
0x01	ChipRev	ChipRev[7:0]*							
0x02	Reserved	Reserved							
0x03	BoostCDiv	**ClkDivEn**	**ClkDivSet[6:0]**						
0x04	BoostISet	—	—	—	—	—	**BoostISet[2:0]**		
0x05	BoostVSet	—	—	—	**BoostVSet[4:0]**				
0x06	BoostCfg	**BoostSeq[2:0]***			BoostEn[1:0]		-	BoostEMI	**BoostInd**
0x07	BuckVSet	—	—	**BuckVSet[5:0]**					
0x08	BuckCfg	**BuckSeq[2:0]***			BuckEn[1:0]		BuckMd[1:0]		**BuckFst**
0x09	BuckISet	**BuckISet[2:0]**			**BuckCfg**	**BuckInd**	**BuckHysOff**	**BuckMinOT**	**BuckInteg**
0x0A	LDOVSet	—	—	—	**LDOVSet[4:0]**				
0x0B	LDOCfg	**LDOSeq[2:0]***			**LDO PasDSC**	**LDO ActDSC**	LDOEn[1:0]		**LDOMode**
0x0C	SwitchCfg	**SWSeq[2:0]***			—	—	SWEn[1:0]		**SWSoftStart**
0x0D	BatTime			**BCVTm[1:0]**		**OCVTm[1:0]**		**LCVTm[1:0]**	
0x0E	BatCfg	BIA**	BIMAbort**	—	—	LcvDly2Skip	**BatImpCur[2:0]**		
0x0F	BatBCV	BCV[7:0]*							
0x10	BatOCV	OCV[7:0]*							
0x11	BatLCV	LCV[7:0]*							
0x12-0x18	Reserved	Reserved							
0x19	MONCfg	MONEn	—	—	—	MONHiZ	MONCtr[2:0]		
0x1A	BootCfg	**PwrRstCfg[3:0]***				**SftRstCfg***	**PFNPUDCfg***	**BootDly[1:0]***	
0x1B	PinStat	—	—	—	—	KIN/SWEN	KOUT/HVEN	MPC/BEN	RST/LEN
0x1C	BBBExtra	**Boost HysOff**	**BoostPasDsc**	**Boost ActDsc**	—	—	**BuckPasDsc**	**BuckActDsc**	**BuckFScl**
0x1D	HandShk	**StartOff***	**GlbPasDsc***	—	—	—	—	—	**StayOn**
0x1E	UVLOCfg	—	—	—	—	—	—	**BBBUVLOsel***	**LDO UVLOsel**
0x1F	PWROFF	PWROFFCMD[7:0]							
0x20… 0x2B	OTPMap	Programmed Default OTP Values							

Note: *All registers reset to default value on hard and soft reset.*
Reserved Bits: Must not be modified from their default states to ensure proper operation.
Bolded Names: Bits default value can be factory configured by OTP. Bolded bits with asterisk are set by OTP only.
**Read-only*
***Bits autoreset at the end of impedance measurement (either completed or aborted).*

I²C Register Descriptions

Table 2. ChipId Register (0x00)

ADDRESS:	0x00 (Read-Only)							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	ChipId[7:0]							
Chip_Id[7:0]	Chip_Id[7:0] bits show information about the version of the MAX14720/MAX14750.							

Table 3. ChipRev Register (0x01)

ADDRESS:	0x01 (Read-Only)							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	ChipRev[7:0]							
ChipRev[7:0]	ChipRev[7:0] bits show information about the revision of the MAX14720/MAX14750 silicon.							

Table 4. BoostCDiv Register (0x03)

ADDRESS:	0x03							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	ClkDivEn	ClkDivSet[6:0]						
ClkDivEn	Boost Current-Limited Output Mode Enable This allows the boost regulator to be operated in a current limited output mode. 0: Normal Operation, Full Output Current Capability 1: Divided Clock Current Limited Mode When the clock divider is enabled, the boost is operated with a fixed peak current limit and programmable frequency. The peak current is set by BoostISet[2:0] and the switching frequency is determined by ClkDivSet[6:0]. The regulator will stop switching when the voltage is above the set point and will only run when the voltage is below the output setting. This mode can only be enabled once the output voltage is set higher than the input voltage.							
ClkDivSet[6:0]	Current-Limited Boost Clock Divider Setting When the current limited mode is enabled, the frequency of the boost regulator in current limited mode will be the frequency of the oscillator divided by the value of (10 + ClkDivSet[6:0]). The range is $f_{OSC}/10$ to $f_{OSC}/137$.							

Table 5. BoostISet Register (0x04)

ADDRESS:	0x04							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	—	—	—	—	—	BoostISet[2:0]		
BoostISet[2:0]	Buck-Boost Peak Current-Limit Setting 000: 0 (Minimum On-Time) 001: 50mA 010: 100mA 011: 150mA 100: 200mA 101: 250mA 110: 300mA 111: 350mA							

Table 6. BoostVSet Register (0x05)

ADDRESS:	**0x05**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	—	—	—	BoostVSet[4:0]				
BoostVSet[4:0]	Boost Output Voltage Setting. This setting is internally latched and can change only when boost is disabled. 2.5V to 5.0V, linear scale, 100mV increments 000000 = 2.5V 000001 = 2.6V … 011001 = 5.0V > 011001 = 5.0V							

Table 7. BoostCfg Register (0x06)

ADDRESS:	**0x06**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	BoostSeq[2:0] (Read-only)			BoostEn[1:0]		—	BoostEMI	BoostInd
BoostSeq[2:0]	Boost Enable Configuration (Read-Only) 000 = Disabled 001 = Reserved 010 = Enabled at 0% of Boot/POR Process Delay Control 011 = Enabled at 25% of Boot/POR Process Delay Control 100 = Enabled at 50% of Boot/POR Process Delay Control 101 = Reserved 110 = Controlled by HVEN (MAX14750) 111 = Controlled by BoostEn [1:0] after 100% of Boot/POR Process Delay Control (MAX14720)							
BoostEn[1:0]	Boost Enable Configuration (effective only when BoostSeq[2:0] == 111) 00 = Disabled. Active discharge behavior depends on BoostActDsc. 01 = Enabled 10 = Enabled when MPC is high 11 = Reserved							
BoostEMI	Boost EMI reduction. Dampens ringing of the inductor when in discontinuous mode 0 = EMI damping active (improve EMI) 1 = EMI damping disabled (improve Efficiency)							
BoostInd	Boost Inductance Select 1 = Inductance is 3.3μH 0 = Inductance is 4.7μH							

Table 8. BuckVSet Register (0x07)

ADDRESS:	0x07							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	—	—	BuckVSet[5:0]					
BuckVSet[5:0]	Buck Output Voltage Setting This setting is internally latched and can change only when buck is disabled. 1.0V to 2.0V, linear scale, 25mV increments 000000 = 1.000V 000001 = 1.025V … 101000 = 2.0V > 101000 = 2.0V							

Table 9. BuckCfg Register (0x08)

ADDRESS:	0x08							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	BuckSeq[2:0] (Read-only)			BuckEn[1:0]		BuckMd[1:0]		BuckFst
BuckSeq[2:0]	Buck Enable Configuration (Read-Only) 000 = Disabled 001 = Reserved 010 = Enabled at 0% of Boot/POR Process Delay Control 011 = Enabled at 25% of Boot/POR Process Delay Control 100 = Enabled at 50% of Boot/POR Process Delay Control 101 = Reserved 110 = Controlled by BEN (MAX14750) 111 = Controlled by BuckEn [1:0] after 100% of Boot/POR Process Delay Control							
BuckEn[1:0]	Buck Enable Configuration (effective only when BuckSeq[2:0] == 111) 00 = Disabled. Active discharge behavior depends on BuckActDsc. 01 = Enabled 10 = Enabled when MPC is high 11 = Reserved							
BuckMd[1:0]	Buck Mode Select 00 = Burst mode 01 = Forced-PWM mode 10 = Forced-PWM mode when MPC is high 11 = Reserved							
BuckFst	Buck Fast Start 0 = Normal startup current limit 1 = Double the startup current to reduce the startup time by half							

Table 10. BuckISet Register (0x09)

ADDRESS:	0x09							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	BuckISet[2:0]			BuckCfg	BuckInd	BuckHysOff	BuckMinOT	BuckInteg
BuckISet[2:0]	Buck Peak Current Limit Setting 000: 50mA 001: 100mA 010: 150mA 011: 200mA 100: 250mA 101: 300mA 110: 350mA 111: 400mA							
BuckCfg	Buck Configuration 0 = Set to 0 for burst mode 1 = Set to 1 for FPWM mode							
BuckInd	Buck Inductance Select 0 = Inductance is 2.2μH 1 = Inductance is 4.7μH							
BuckHysOff	Buck Hysteresis Off 0 = Enable comparator hysteresis 1 = Disable comparator hysteresis (recommended to reduce voltage ripple)							
BuckMinOT	Buck Minimum On-Time 0 = Enable deglitch delay on comparator for better efficiency 1 = Disable deglitch delay on comparator to minimize voltage ripple							
BuckInteg	Buck Integrate 0 = Helps stabilize the buck regulator for high currents with small output capacitor 1 = Better load regulation at high current (recommended for output capacitance > 6μF)							

Table 11. LDOVSet Register (0x0A)

ADDRESS:	0x0A							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME				LDOVSet[4:0]				
LDOVSet[4:0]	LDO Output Voltage Setting 0.9V to 4V, linear scale, 100mV increments 00000 = 0.9V 00001 = 1.0V … 10000 = 2.5V … 11111 = 4.0V							

Table 12. LDOCfg Register (0x0B)

ADDRESS:	0x0B							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	LDOSeq[2:0] (Read-Only)			LDOPasDsc	LDOActDsc	LDOEn[1:0]		LDOMode
LDOSeq[2:0]	LDO Enable Configuration (Read-Only) 000 = Disabled 001 = Enabled always when BAT/SYS is present 010 = Enabled at 0% of Boot/POR Process Delay Control 011 = Enabled at 25% of Boot/POR Process Delay Control 100 = Enabled at 50% of Boot/POR Process Delay Control 101 = Disabled 110 = Controlled by LEN (MAX14750) 111 = Controlled by LDOEn[1:0] after 100% of Boot/POR Process Delay Control							
LDOPasDsc	LDO Passive Discharge Control 0: LDO output will be discharged only entering off and hard-reset modes. 1: LDO output will be discharged only entering off and hard-reset modes and when the enable is low.							
LDOActDsc	LDO Active Discharge Control 0: LDO output will be actively discharged only entering off and hard-reset modes. 1: LDO output will be actively discharged only entering off and hard-reset modes and when the enable is low.							
LDOEn[1:0]	LDO Enable Configuration (effective only when LDOSeq[2:0] == 111) 00 = Disabled 01 = Enabled 10 = Enabled when MPC is high 11 = Reserved							
LDOMode	LDO Mode Control 0 = Normal LDO operating mode 1 = Load switch mode. FET is either fully on or off depending on the state of LDOEn. When FET is on, the output is unregulated and is not affected by UVLO’s control block. This setting is internally latched and can change only when the LDO is disabled.							

Table 13. SwitchCfg Register (0x0C)

ADDRESS:	0x0C							
BIT	7	6	5	4	3	2	1	0
NAME	SWSeq[2:0] (Read-Only)			—	—	SWEn[1:0]		SWSoftStart
SWSeq[2:0]	SW Enable Configuration (Read-Only) 000 = Disabled 001 = Enabled always when BAT/SYS is present 010 = Enabled at 0% of Boot/POR Process Delay Control 011 = Enabled at 25% of Boot/POR Process Delay Control 100 = Enabled at 50% of Boot/POR Process Delay Control 101 = Disabled 110 = Controlled by SWEN (MAX14750) 111 = Controlled by SWEn[1:0] after 100% of Boot/POR Process Delay Control							
SWEn	SW Enable Configuration (effective only when SWSeq[2:0] == 111) 00 = Disabled 01 = Enabled 10 = Enabled when MPC is high 11 = Reserved							
SWSoftStart	SW Soft-Start 0 = No soft-start is present when the switch is enabled. 1 = Current limit of 25mA (typ) is ensured for 60ms when the switch is enabled.							

Table 14. BatTime Register (0x0D)

ADDRESS:	0x0D							
BIT	7	6	5	4	3	2	1	0
NAME	—	—	BCVTm[1:0]		OCVTm[1:0]		LCVTm[1:0]	
BCVTm[1:0]	Battery Cell Voltage Timing 00: Skip battery measurement 01: Take battery measurement after 10ms delay 10: Take battery measurement after 100ms delay 11: Take battery measurement after 1000ms delay							
OCVTm[1:0]	Battery Open Cell Voltage Timing If this step is skipped, LCV measurement will be taken with switch closed 00: Skip OCV measurement 01: Take OCV measurement after 10ms delay 10: Take OCV measurement after 100ms delay 11: Take OCV measurement after 1000ms delay							
LCVTm[1:0]	Battery Loaded Cell Voltage Timing 00: Skip LCV measurement 01: Take LCV measurement after 10ms delay 10: Take LCV measurement after 100ms delay 11: Take LCV measurement after 1000ms delay							

Table 15. BatCfg Register (0x0E)

ADDRESS:	0x0E							
BIT	7	6	5	4	3	2	1	0
NAME	BIA	BIMAbort	—	—	LcvDly2Skip	BatImpCur[2:0]		
BIA	Battery Impedance Active Write 1 to start battery impedance measurement. If the measurement is already running, the write is ignored. Bit will remain high until the measurement is completed. 0: Battery impedance measurement is not ongoing 1: Battery impedance measurement is ongoing							
BIMAbort	Battery Impedance Measurement Skip Write 1 to immediately abort the battery impedance measurement 0: Battery impedance measurement is aborted 1: Battery impedance measurement is not aborted yet							
LcvDly2Skip	Write 1 to skip the second delay time (equal again to LCVTm) after LCV Measurement is taken. This second delay time allows V_{CC} to recover its unloaded value before closing the power switch again. 0: Wait second delay time 1: Skip second delay time							
BatImpCur [2:0]	Battery Impedance Current 000: 0 001: 250μA 010: 500μA 011: 1mA 100: 2mA 101: 4mA 110: 8mA 111: Reserved							

Table 16. BatV Register (0x0F)

ADDRESS:	0x0F (Read-Only)							
BIT	7	6	5	4	3	2	1	0
NAME	BCV[7:0]							
BCV[7:0]	Battery Voltage Measurement Result 8-bit battery voltage measurement: V_{CC} = [2.6 * (BCV[7:0]/255) + 1.1] V If BCVTm[2:0] = 00, BCV[7:0] = 0000 0000. If error occurs or the measurement is aborted, BCV[7:0] =1111 1111.							

Table 17. BatOCV Register (0x10)

ADDRESS:	0x10 (Read-Only)							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	OCV[7:0]							
OCV[7:0]	Battery Voltage Measurement Result 8-bit battery voltage measurement: V_{CC} = [2.6 x (OCV[7:0]/255) + 1.1] V If OCVTm[2:0] = 00, OCV[7:0] =0000 0000. If error occurs or the measurement is aborted, OCV[7:0] =1111 1111.							

Table 18. BatLCV Register (0x11)

ADDRESS:	0x11 (Read-Only)							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	LCV[7:0]							
LCV[7:0]	Battery Voltage Measurement Result 8 bit battery voltage measurement: V_{CC} = [2.6 x (LCV[7:0]/255) + 1.1] V If LCVTm[2:0] = 00, BCV[7:0] = 0000 0000. If error occurs or the measurement is aborted, LCV[7:0] =1111 1111.							

Table 19. MONCfg Register (0x19)

ADDRESS:	0x19							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	MonEn	—	—	—	MONtHiZ	MONCtr[2:0]		
MonEn	Monitor Enable 0 = Monitor function disabled 1 = Monitor function enabled							
MONtHiZ	MON OFF MODE Condition 0 = Pulled Low by a 100k Pulldown Resistor 1 = Hi-Z							
MONCtr[2:0]	MON Pin Source Selection 000 = MON connected to SWIN 001 = MON connected to SWOUT 010 = MON connected to BIN 011 = MON connected to BOUT 100 = MON connected to HVIN 101 = MON connected to HVOUT 110 = MON connected to LIN 111 = MON connected to LOUT							

Table 20. BootCfg Register (0x1A)

ADDRESS:	**0x1A (Read-Only)**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	PwrRstCfg[4:0]				SftRstCfg	PFNPUDCfg	BootDly[1:0]	
PwrRstCfg [4:0]	0000: Pin Controlled (MAX14750) 0110: Push-Button Monitor (MAX14720)							
SftRstCfg	Soft-Reset Register Default 0 = Registers do not reset to default values on soft reset 1 = Registers reset to default values on soft reset							
PFNPUDCfg	KIN Pullup/Pulldown Configuration 0 = Pullups and pulldowns on control lines disabled 1 = Selective pullups and pulldowns enabled on KIN pin							
BootDly[1:0]	Boot/POR Process t_{RESET} Delay Control 00 = 80ms 01 = 120ms 10 = 220ms 11 = 420ms							

Table 21. PinStat Register (0x1B)

ADDRESS:	**0x1B (Read-Only)**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME (MAX14720)	—	—	—	—	$\overline{\text{KIN}}$	$\overline{\text{KOUT}}$	MPC	$\overline{\text{RST}}$
NAME (MAX14750)	—	—	—	—	SWEN	HVEN	BEN	LEN
$\overline{\text{KIN}}$, $\overline{\text{KOUT}}$, MPC, $\overline{\text{RST}}$, SWEN, HVEN, BEN, LEN	Input State 0 = Pin low 1 = Pin high							

Table 22. BBBExtra Register (0x1C)

ADDRESS:	0x1C							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	BoostHysOff	BoostPasDsc	BoostActDsc	-	0	BuckPasDsc	BuckActDsc	BuckFScl
BoostHysOff	Boost Hysteresis Off 0 = Enable comparator hysteresis 1 = Disable comparator hysteresis (recommended to reduce voltage ripple)							
BoostPasDsc	Boost Passive Discharge Control 0: Boost output will be discharged only when entering off and hard-reset modes. 1: Boost output will be discharged only when entering off and hard-reset modes and when BoostEn is set to 00.							
BoostActDsc	Boost Active Discharge Control 0: Boost output will be discharged only when entering off and hard-reset modes. 1: Boost output will be discharged only when entering off and hard-reset modes and when BoostEn is set to 00.							
BuckPasDsc	Buck Passive Discharge Control 0: Buck output will be discharged only when entering off and hard-reset modes. 1: Buck output will be discharged only when entering off and hard-reset modes and when BuckEn is set to 00.							
BuckActDsc	Buck Active Discharge Control 0: Buck output will be discharged only when entering off and hard-reset modes. 1: Buck output will be discharged only when entering off and hard-reset modes and when BuckEn is set to 00.							
BuckFScl	Buck Force FET scaling (it reduces I_Q by lowering the nMOS power to 20% of the nominal value) 0: FET Scaling only enabled during the buck turn-on sequence 1: FET Scaling enabled during the buck turn-on sequence and also in the buck active state.							

Table 23. HandShk Register (0x1D)

ADDRESS:	0x1D (Read-Only)							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	StartOff	GlbPasDsc	—	—	—	—	—	StayOn
StartOff	Start In Off 1: The device will start in the off mode. 0: The device begins the power-on sequence after a V_{CC} power on reset.							
GlbPasDsc	Global Passive Discharge 0: Passive discharge loads are disabled in off mode. 1: Passive discharge loads are enabled in off mode.							
StayOn	Processor Handshake This bit is used to ensure that the processor booted correctly. This bit must be set within 5s of power-on to prevent the part from shutting down and returning to the power-off condition. This bit has no effect after being set. 0 = Shutdown 5s after power-on 1 = Stay on							

Table 24. UVLOCfg Register (0x1E)

ADDRESS:	**0x1E**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	—	—	—	—	—	—	BBBUVLOsel (Read Only)	LDOUVLOsel
BBBUVLOsel	Buck/Buck-Boost UVLO Select 0: Buck and buck-boost are turned off/on according to LIN_UVLO thresholds 1: Buck and buck-boost are turned off/on according to BIN_UVLO thresholds							
LDOUVLOsel	LDO UVLO Select 0: LDO is turned off/on according to LIN_UVLO thresholds 1: LDO is turned off/on according to BIN_UVLO thresholds							

Table 25. PWRCFG Register (0x1F)

ADDRESS:	**0x1F**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	PWROFFCMD[7:0]							
PWROFFCMD [7:0]	Power-Off Command Writing 0xB2 to this register will place the part in the off state/seal mode. Waking up the device from this mode requires a low pulse on $\overline{KIN}$. All other codes = Do nothing							

I²C Interface

The MAX14720/MAX14750 contain an I²C-compatible interface for data communication with a host controller (SCL and SDA). The interface supports a clock frequency of up to 400kHz. SCL and SDA require pullup resistors that are connected to a positive supply.

Start, Stop, And Repeated Start Conditions

When writing to the MAX14720/MAX14750 using I²C, the master sends a START condition (S) followed by the MAX14720/MAX14750 I²C address. After the address, the master sends the register address of the register that is to be programmed. The master then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a REPEATED START condition (Sr) to communicate to another I²C slave. See Figure 4.

Table 26. I²C Slave Addresses

ADDRESS FORMAT	HEX	BINARY
7-Bit Slave ID	0x2A	0101010
Write Address	0x54	0000 0100
Read Address	0x55	01010101

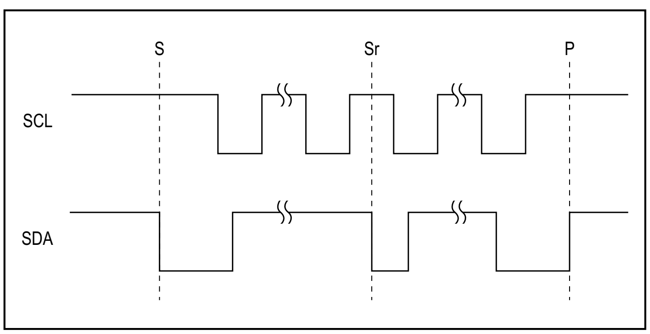


Figure 4. I²C START, STOP, and REPEATED START Conditions

Slave Address

Set the Read/$\overline{\text{Write}}$ bit high to configure the devices to read mode (Table 26). Set the Read/$\overline{\text{Write}}$ bit low to configure the MAX14720/MAX14750 to write mode. The address is the first byte of information sent to the MAX14720/MAX14750 after the START condition.

Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the *Start, Stop, And Repeated Start Conditions* section). Both SDA and SCL remain high when the bus is not active.

Single-Byte Write

In this operation, the master sends an address and two data bytes to the slave device (Figure 5). The following procedure describes the single byte write operation:

1) The master sends a START condition
2) The master sends the 7-bit slave address plus a write bit (low)
3) The addressed slave asserts an ACK on the data line
4) The master sends the 8-bit register address
5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
6) The master sends 8 data bits
7) The slave asserts an ACK on the data line
8) The master generates a STOP condition

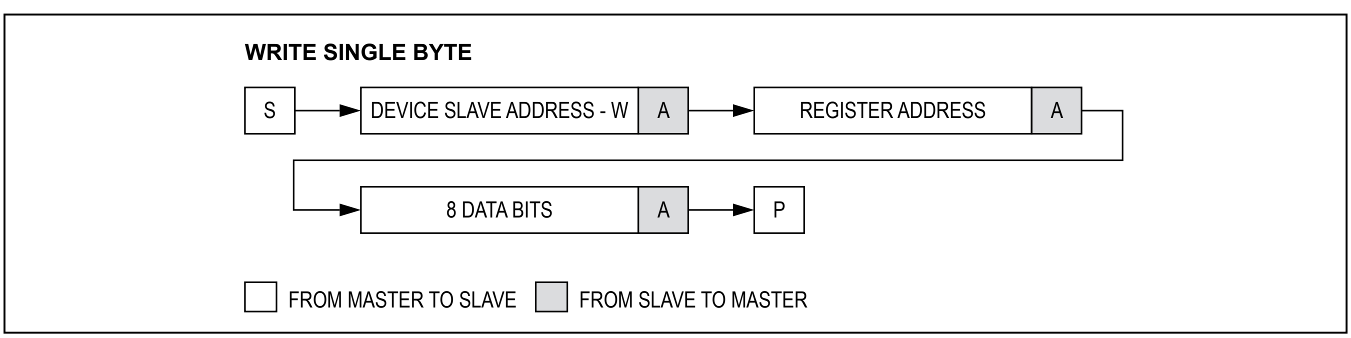


Figure 5. Write Byte Sequence

Burst Write

In this operation, the master sends an address and multiple data bytes to the slave device (Figure 6). The slave device automatically increments the register address after each data byte is sent, unless the register being accessed is 0x00, in which case the register address remains the same. The following procedure describes the burst write operation:

1) The master sends a START condition
2) The master sends the 7-bit slave address plus a write bit (low)
3) The addressed slave asserts an ACK on the data line
4) The master sends the 8-bit register address
5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
6) The master sends eight data bits
7) The slave asserts an ACK on the data line
8) Repeat 6 and 7 N-1 times
9) The master generates a STOP condition

Single Byte Read

In this operation, the master sends an address plus two data bytes and receives one data byte from the slave device (I2C Register Descriptions). The following procedure describes the single byte read operation:

1) The master sends a START condition.
2) The master sends the 7-bit slave address plus a write bit (low).
3) The addressed slave asserts an ACK on the data line.
4) The master sends the 8-bit register address.
5) The slave asserts an ACK on the data line only if the address is valid (NAK if not).
6) The master sends a REPEATED START condition.
7) The master sends the 7-bit slave address plus a read bit (high).
8) The addressed slave asserts an ACK on the data line.
9) The slave sends eight data bits.
10) The master asserts a NACK on the data line.
11) The master generates a STOP condition.

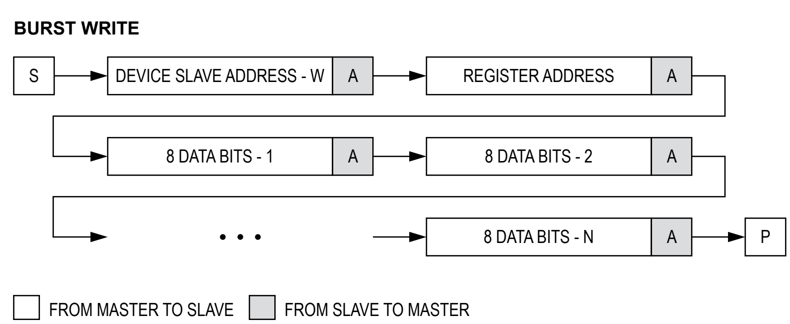


Figure 6. Burst Write Sequence

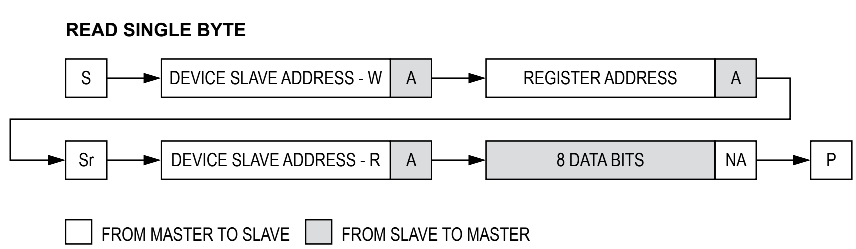


Figure 7. Read Byte Sequence

Burst Read

In this operation, the master sends an address plus two data bytes and receives multiple data bytes from the slave device (Figure 8). The following procedure describes the burst byte read operation:

1) The master sends a START condition
2) The master sends the 7-bit slave address plus a write bit (low)
3) The addressed slave asserts an ACK on the data line
4) The master sends the 8-bit register address
5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
6) The master sends a REPEATED START condition
7) The master sends the 7-bit slave address plus a read bit (high)
8) The slave asserts an ACK on the data line
9) The slave sends eight data bits
10) The master asserts an ACK on the data line
11) Repeat 9 and 10 N-2 times
12) The slave sends the last eight data bits
13) The master asserts a NACK on the data line
14) The master generates a STOP condition

Acknowledge Bits

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX14720/MAX14750 generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse (Figure 9). To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows for detection of unsuccessful data transfers.

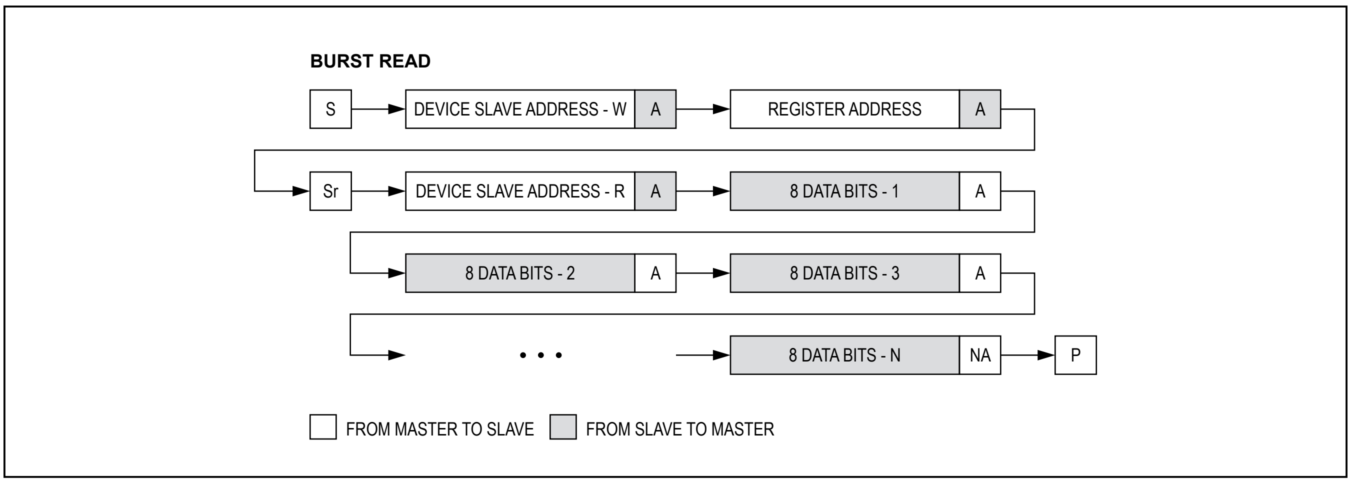


Figure 8. Burst Read Sequence

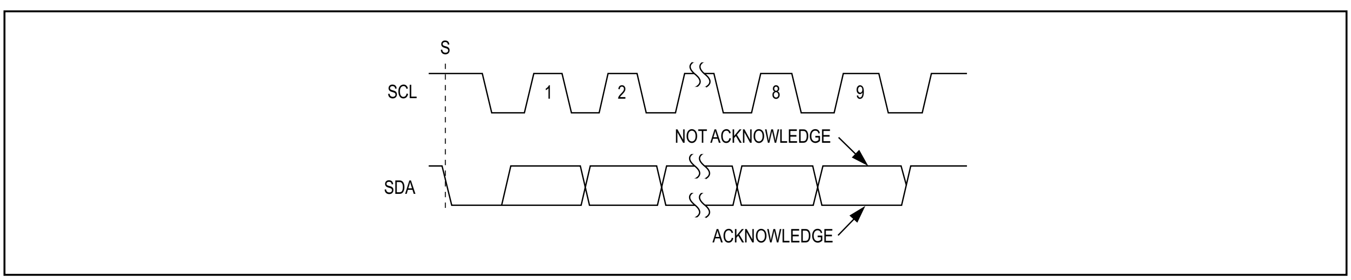


Figure 9. Acknowledge

Table 27. Register Bit Default Values

REGISTER BITS	MAX14750A	MAX14750B	MAX14720A	MAX14720B	MAX14720C	MAX14720D
BoostISet[2:0]	100mA	100mA	100mA	100mA	150mA	100mA
BoostVSet[4:0]	3.3V	3.3V	3.3V	3.3V	3.5V	3.3V
BBBUVLOSel	BIN	BIN	BIN	BIN	BIN	BIN
LDOUVLOSel	LIN	LIN	BIN	BIN	LIN	LIN
BuckVSet[5:0]	1.2V	1.8V	1.2V	1.8V	1.2V	1.8V
BuckISet[2:0]	300mA	300mA	300mA	300mA	50mA	150mA
BuckCfg	Burst	Burst	Burst	Burst	Burst	Burst
BuckInd	2.2µH	2.2µH	2.2µH	2.2µH	2.2µH	2.2µH
BuckHysOff	Lower Ripple	Lower Ripple	Lower Ripple	Lower Ripple	Lower Ripple	Lower Ripple
BuckMinOT	Lower Ripple	Lower Ripple	Lower Ripple	Lower Ripple	Lower Ripple	Lower Ripple
BuckInteg	Higher DC Accuracy	Higher DC Accuracy	Higher DC Accuracy	Higher DC Accuracy	Higher DC Accuracy	Higher DC Accuracy
I2CAdd	0101010	0101010	0101010	0101011	0101010	0101011
StayOn	Stay On	Stay On	Stay On	Stay On	Off after 5s	Stay On
LDOVSet[4:0]	1.8V	1.2V	1.8V	1.8V	1.8V	1.8V
BoostSeq[2:0]	HVEN	HVEN	BoostEn (I2C)	BoostEn (I2C)	BoostEn (I2C)	BoostEn (I2C)
BoostInd	4.7µH	4.7µH	4.7µH	4.7µH	4.7µH	4.7µH
BuckSeq[2:0]	BEN	BEN	50%	50%	25%	50%
BuckFst	Zero	Zero	Zero	Zero	Zero	Zero
LDOSeq[2:0]	LEN	LEN	50%	LDOEn (I^2C)	50%	Always
LDOMode	LDO	LDO	LDO	Load Switch	LDO	LDO
SWSeq[2:0]	SWEN	SWEN	0%	0%	0%	0%
SWSoftStart	None	None	25mA (typ) for 60ms	25mA (typ) for 60ms	20mA (typ) for 60ms	20mA (typ) for 60ms
BCVTm[1:0]	Skip	Skip	Skip	Skip	Skip	Skip
OCVTm[1:0]	Skip	Skip	Skip	Skip	Skip	Skip
LCVTm[1:0]	Skip	Skip	Skip	Skip	Skip	Skip
LDOPasDSC	Off	Off	Off	Off	Off	Off
LDOActDSC	Off	Off	Off	Off	Off	Off
BatImpCur	0mA	0mA	0mA	0mA	0mA	0mA
PwrRstCfg[3:0]	Pin Enable	Pin Enable	$\overline{KIN}$	$\overline{KIN}$	$\overline{KIN}$	$\overline{KIN}$
SftRstCfg	Hold Regs	Hold Regs	Hold Regs	Hold Regs	Hold Regs	Hold Regs
PFNPUDCfg	Disabled	Disabled	Enabled	Enabled	Enabled	Enabled
BootDly[1:0]	80ms	80ms	120ms	120ms	220ms	120ms
StartOff	Power On	Power On	Remain Off	Remain Off	Power On	Remain Off
GlbPasDsc	Disabled	Disabled	Disabled	Disabled	Enabled	Disabled
BoostHysOff	More Efficient	More efficient	More Efficient	More Efficient	More efficient	More efficient

Table 27. Register Bit Default Values (continued)

REGISTER BITS	MAX14750A	MAX14750B	MAX14720A	MAX14720B	MAX14720C	MAX14720D
BoostPasDsc	Off	Off	Off	Off	Off	Off
BoostActDsc	Off	Off	Off	Off	Off	Off
BuckPasDsc	Off	Off	Off	Off	Off	Off
BuckActDsc	Off	Off	Off	Off	Off	Off
BuckFScl	Zero	Zero	Zero	Zero	Zero	Zero
ClkDivEna	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
ClkDivSet[6:0]	0	0	0	0	0	0

Table 28. Register Default Values

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUES					
		MAX14750A	MAX14750B	MAX14720A	MAX14720B	MAX14720C	MAX14720D
0x00	ChipId	0x01	0x01	0x01	0x01	0x01	0x01
0x01	ChipRev	0x01	0x01	0x01	0x01	0x01	0x01
0x02	Reserved	0x00	0x00	0x00	0x00	0x00	0x00
0x03	BoostCDiv	0x00	0x00	0x00	0x00	0x00	0x00
0x04	BoostISet	0x02	0x02	0x02	0x02	0x03	0x02
0x05	BoostVSet	0x08	0x08	0x08	0x08	0x0A	0x08
0x06	BoostCfg	0xC0	0xC0	0xE0	0xE0	0xE0	0xE0
0x07	BuckVSet	0x08	0x20	0x08	0x20	0x08	0x20
0x08	BuckCfg	0xC0	0xC0	0x80	0x80	0x60	0x80
0x09	BuckISet	0xA7	0xA7	0xA7	0xA7	0x07	0x47
0x0A	LDOVSet	0x09	0x03	0x09	0x09	0x09	0x09
0x0B	LDOCfg	0xC0	0xC0	0x80	0xE1	0x80	0x20
0x0C	SwitchCfg	0xC0	0xC0	0x41	0x41	0x41	0x41
0x0D	BatTime	0x00	0x00	0x00	0x00	0x00	0x00
0x0E	BatCfg	0x00	0x00	0x00	0x00	0x00	0x00
0x0F	BatBCV	0x00	0x00	0x00	0x00	0x00	0x00
0x10	BatOCV	0x00	0x00	0x00	0x00	0x00	0x00
0x11	BatLCV	0x00	0x00	0x00	0x00	0x00	0x00
0x12	Reserved	0x00	0x00	0x00	0x00	0x00	0x00
0x13	Reserved	0x00	0x00	0x00	0x00	0x00	0x00
0x14	Reserved	0x00	0x00	0x00	0x00	0x00	0x00
0x15	Reserved	0x00	0x00	0x00	0x00	0x00	0x00
0x16	Reserved	0x00	0x00	0x00	0x00	0x00	0x00
0x17	Reserved	0x00	0x00	0x00	0x00	0x00	0x00
0x18	Reserved	0x34	0x34	0x34	0x34	0x34	0x34

Table 28. Register Default Values (continued)

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUES					
		MAX14750A	MAX14750B	MAX14720A	MAX14720B	MAX14720C	MAX14720D
0x19	MONCfg	0x00	0x00	0x00	0x00	0x00	0x00
0x1A	BootCfg	0x00	0x00	0x65	0x65	0x66	0x65
0x1B	PinStat	0x00	0x00	0x00	0x00	0x00	0x00
0x1C	BBBExtra	0x00	0x00	0x00	0x00	0x00	0x00
0x1D	HandShk	0x01	0x01	0x81	0x81	0x40	0x81
0x1E	UVLOCfg	0x02	0x02	0x03	0x03	0x02	0x02
0x1F	PWROFF	0x00	0x00	0x00	0x00	0x00	0x00

Typical Application Circuits

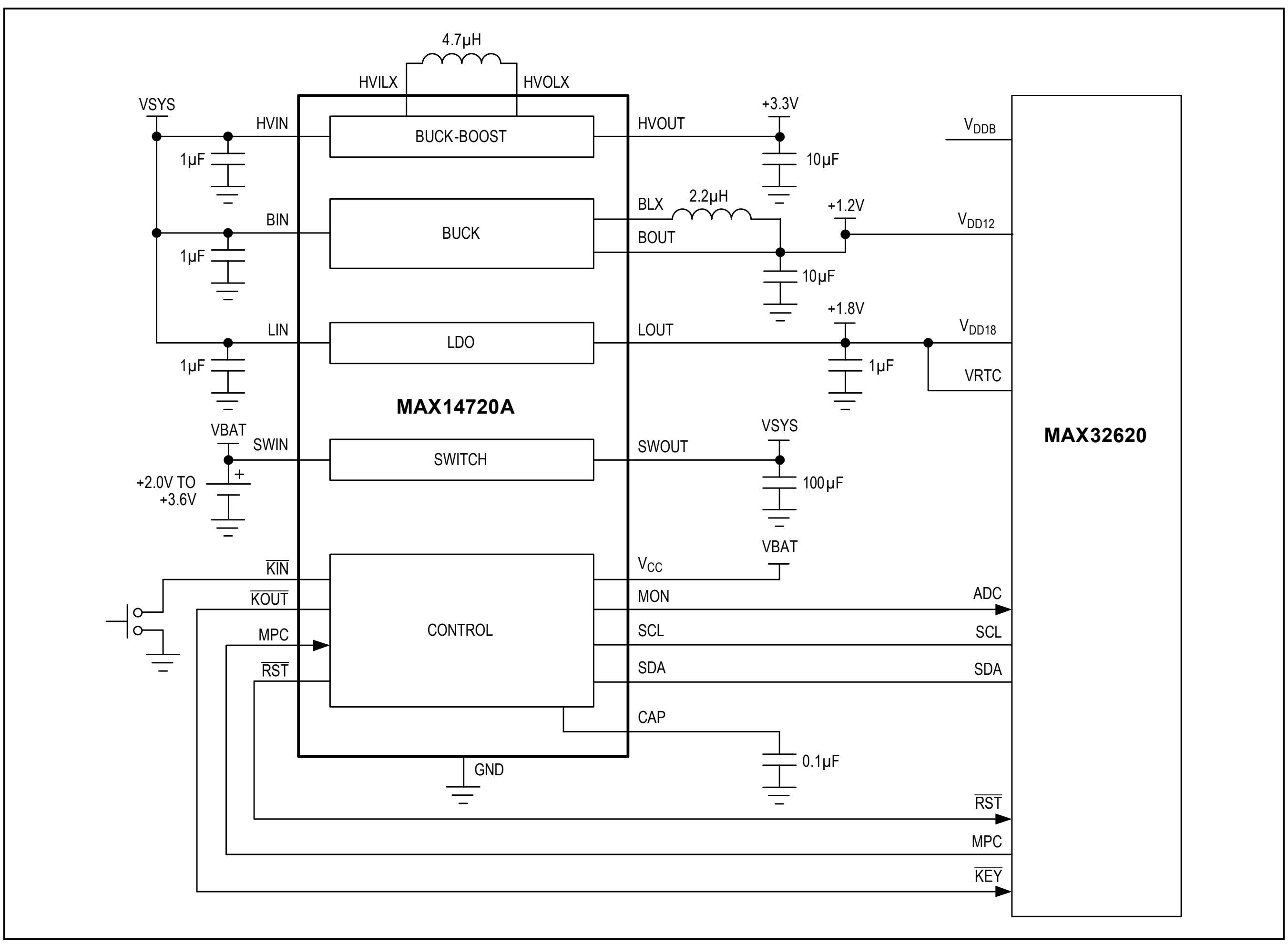


Figure 10. Lithium Coin Cell

Typical Application Circuits (continued)

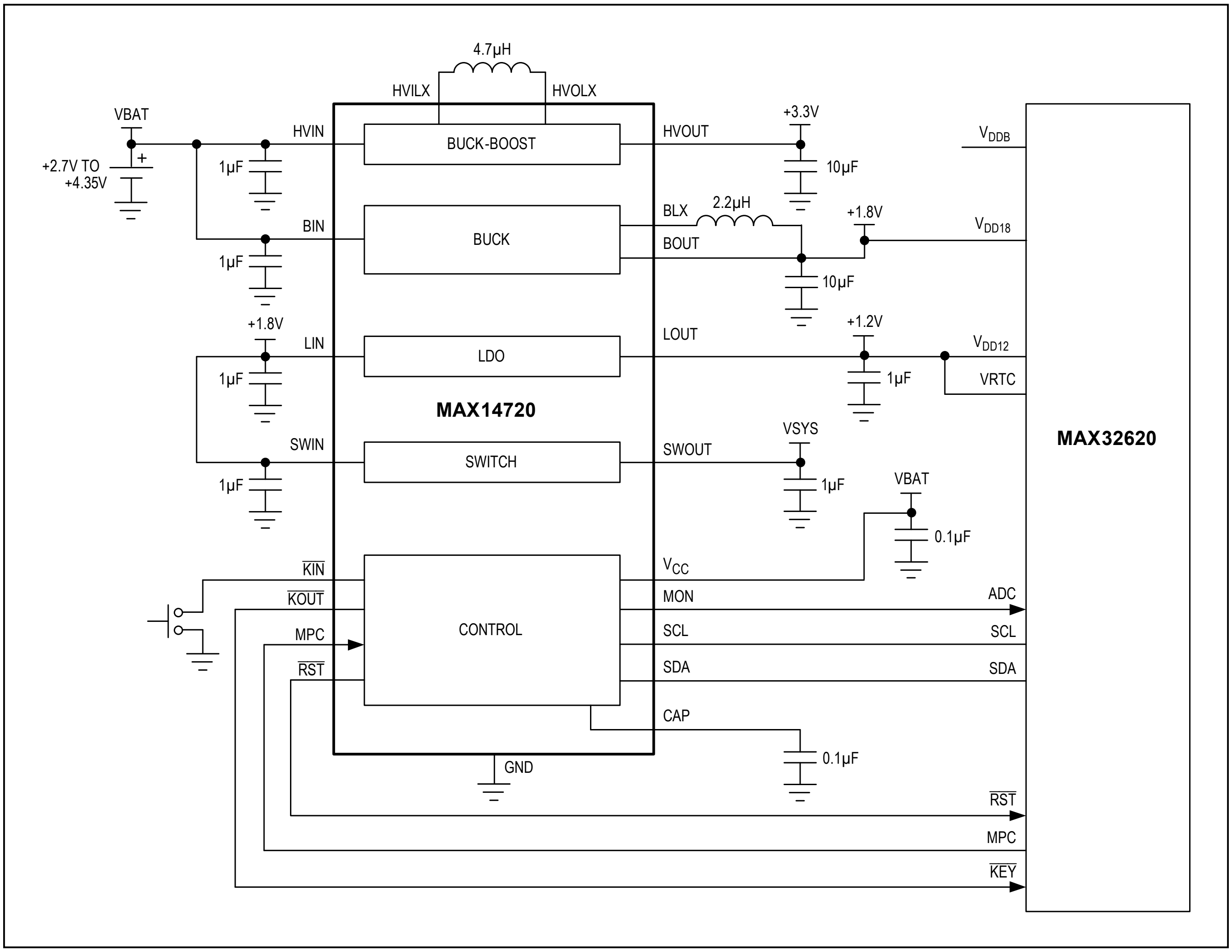


Figure 11. Removable Li+ Rechargeable

Typical Application Circuits (continued)

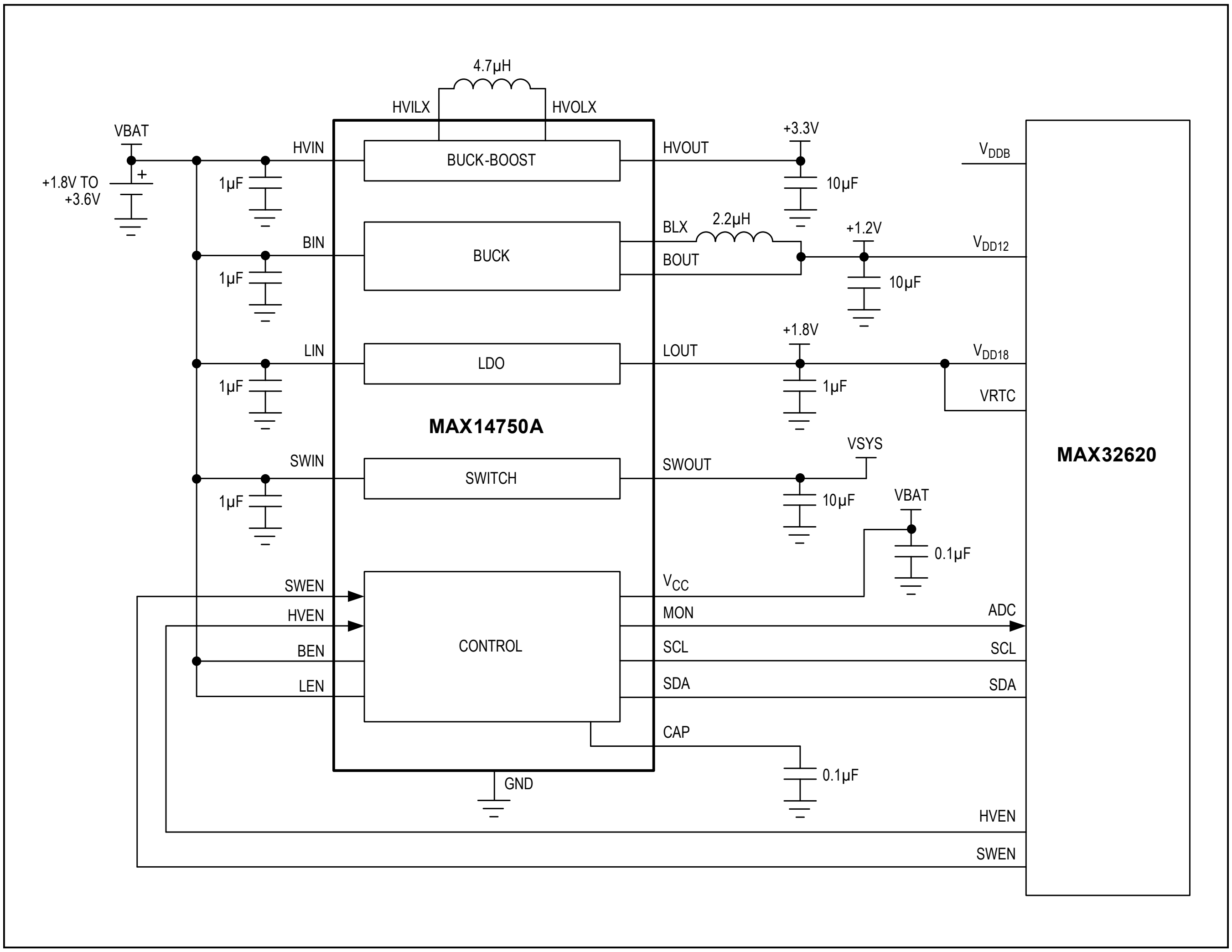


Figure 12. Always-On Coin Cell

Typical Application Circuits (continued)

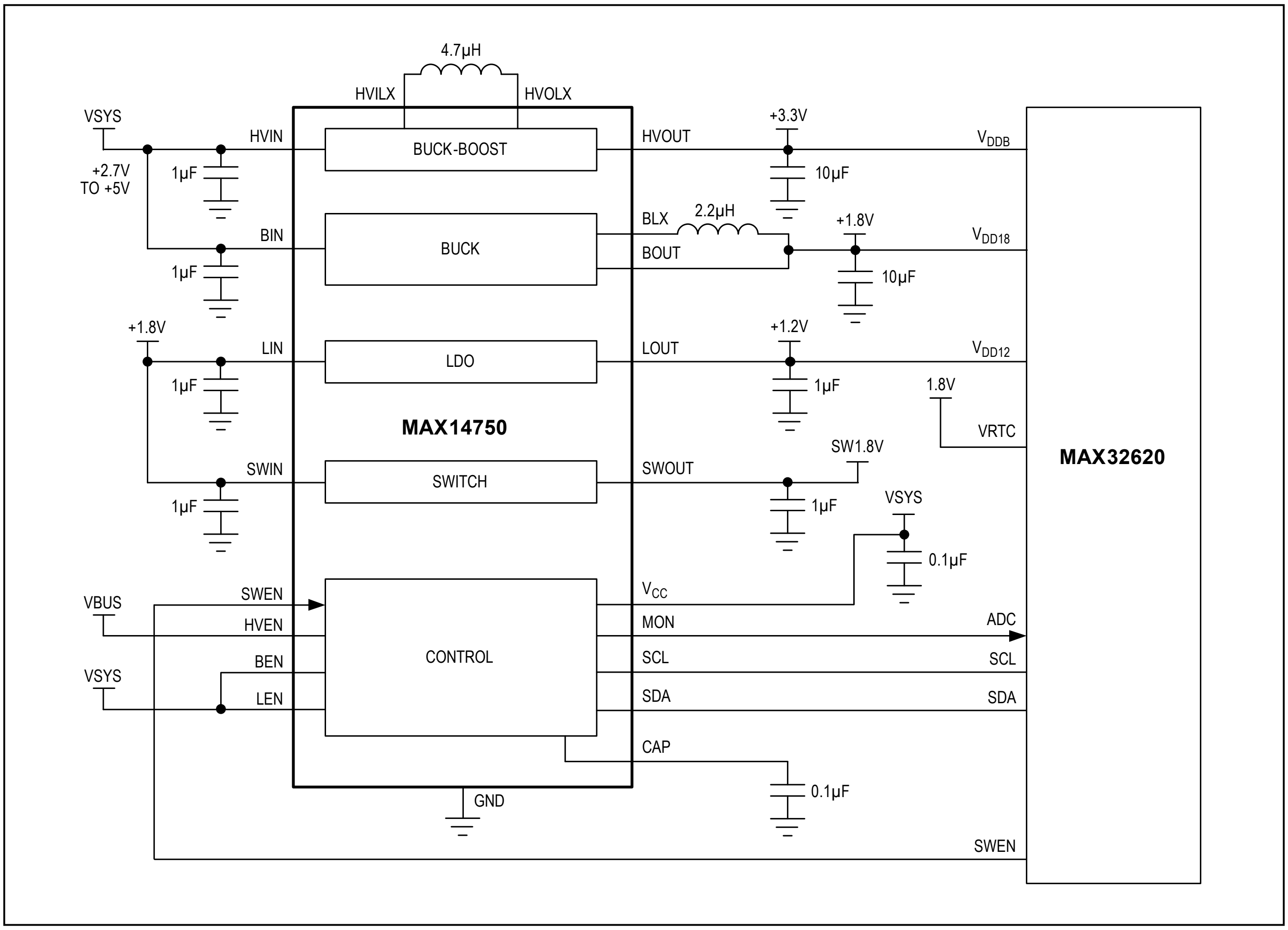


Figure 13. Companion Li+ Rechargeable

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14720AEWA+	-40°C to +85°C	25 WLP
MAX14720AEWA+T	-40°C to +85°C	25 WLP
MAX14720BEWA+*	-40°C to +85°C	25 WLP
MAX14720BEWA+T*	-40°C to +85°C	25 WLP
MAX14720CEWA+	-40°C to +85°C	25 WLP
MAX14720CEWA+T	-40°C to +85°C	25 WLP
MAX14720DEWA+	-40°C to +85°C	25 WLP
MAX14720DEWA+T	-40°C to +85°C	25 WLP
MAX14750AEWA+	-40°C to +85°C	25 WLP
MAX14750AEWA+T	-40°C to +85°C	25 WLP
MAX14750BEWA+*	-40°C to +85°C	25 WLP
MAX14750BEWA+T*	-40°C to +85°C	25 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**Future product—contact factory for availability.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
25 WLP	W252M2+1	**21-0788**	Refer to **Application Note 1891**

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/15	Initial release	—
1	2/16	*Worst-Case Accuracy of Single* V_{CC} *Measurement* spec updated in *Electrical Characteristics* table	8
2	8/16	General updates	16, 21, 31–33
3	3/17	Updated Table 27, Table 28, and updated *Ordering Informaiton* table	31–33, 37
4	5/17	Removed future product designations for MAX14720CEWA+, MAX14720CEWA+T, MAX14720DEWA+, and MAX14720DEWA+T in *Ordering Informaiton* table	37

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

