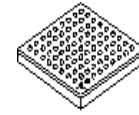




MCIMX25



Package Information
 Plastic package
 Case 5284 17 x 17 mm, 0.8 mm Pitch

i.MX25 Multimedia Applications Processor for Automotive Products

Silicon Version 1.1

| Ordering Information |
|---|
| See Table 1 on page 3 for ordering information. |

1 Introduction

The i.MX25 family of processors offers integration that tailors itself to the connectivity requirements of today's automobile infotainment systems. It has been architected to include auto infotainment requirements like CAN, USB connectivity and audio connectivity, without many of the extra features only needed for high end applications. As a result, the i.MX25 enables many of the features only available in high end systems, but at a price point suitable for all vehicles.

At the core of the i.MX25 is Freescale's fast, proven, power-efficient implementation of the ARM926EJ-S core, with speeds of up to 400 MHz. The i.MX25 includes support for up to 133 MHz DDR2 memory, integrated 10/100 Ethernet MAC, and two on-chip USB PHYs. The automotive versions of the i.MX25 offer AEC-Q100 grade 3 qualification to meet stringent automotive quality

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requirements. The device is suitable for a wide range of applications, including the following:

- USB connectivity
- Audio streaming
- Portable media player connectivity and playback with MP3, AAC, and WMA software support
- External bluetooth control
- Basic voice command & control
- Secure black box
- Smart toll collection

Features of the i.MX25 processor include the following:

- **Advanced power management**—The heart of the device is a level of power management throughout the IC that enables the multimedia features and peripherals to achieve minimum system power consumption in both active and various low-power modes. Power management techniques allow the designer to deliver a feature-rich product that requires levels of power that are far lower than typical industry expectations.
- **Multimedia powerhouse**—The multimedia performance of the i.MX25 processor is boosted by a 16 KB L1 instruction and data cache system, and further enhanced by an LCD controller (with alpha blending), CMOS image sensor interface, A/D controller (integrated touchscreen controller), and a programmable smart DMA (SDMA) controller.
- **128 Kbytes on-chip SRAM**—The additional 128 Kbyte on-chip SRAM makes the device ideal for eliminating external RAM in applications with small footprint RTOS. The on-chip SRAM allows the designer to enable an ultra low power LCD refresh.
- **Interface flexibility**—The device interface supports connection to all common types of external memories: MobileDDR, DDR, DDR2, NOR Flash, PSRAM, SDRAM and SRAM, NAND Flash, and managed NAND/moviNAND™ (via the enhanced secured digital host controller (eSDHC)). Designers seeking to provide products that deliver a rich multimedia experience will find a full suite of on-chip peripherals: LCD controller and CMOS sensor interface, A/D controller (integrated touchscreen controller), parallel ATA, USB 2.0 high-speed on-the-go and full-speed host PHYs, multiple expansion card ports (high-speed MMC/SDIO host and others), fast Ethernet controller, and a variety of other common interfaces including UART, CSPI, I2C, FlexCAN, and SIM card.
- **Increased security**—Because the need for advanced security for tethered and untethered devices continues to increase, the i.MX25 processor delivers hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, robust tamper detection, secure boot, and secure software downloads.
- **On-chip PHY**—The device includes an HS USB OTG PHY and FS USB PHY.
- **Fast Ethernet**—For rapid external communication a fast Ethernet controller (FEC) is included.

1.1 Ordering Information

Table 1 provides the ordering information for the i.MX25.

Table 1. Non-Production Engineering Ordering Information

| Part Number | Silicon Version | Projected Temperature Range (°C) | Package |
|--------------|-----------------|----------------------------------|--------------------------------------|
| MCIMX251AVM4 | 1.1 | -40 to +85 | 17 x 17 mm, 0.8 mm pitch, MAPBGA-400 |
| MCIMX255AVM4 | 1.1 | -40 to +85 | 17 x 17 mm, 0.8 mm pitch, MAPBGA-400 |

1.2 Block Diagram

Figure 1 shows the i.MX25 simplified interface block diagram.

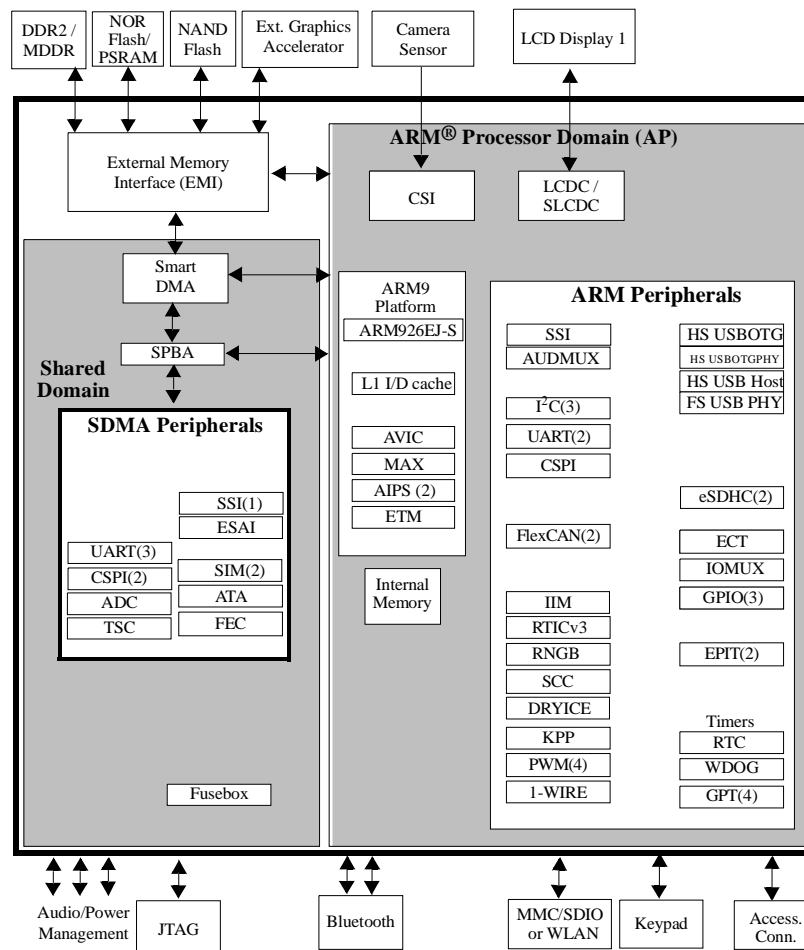


Figure 1. i.MX25 Simplified Interface Block Diagram

2 Features

Table 2 describes the digital and analog modules of the device.

Table 2. i.MX25 Digital and Analog Modules

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|----------------|--|--------------------------|---|
| 1-WIRE | 1-Wire Interface | Connectivity peripherals | 1-Wire support provided for interfacing with an on-board EEPROM, and smart battery interfaces, for example: Dallas DS2502. |
| ARM9 or ARM926 | ARM926 platform and memory | ARM® | The ARM926 Platform consists of the ARM926EJ-S™ core, the ETM real-time debug modules, a 5x5 Multi-Layer AHB crossbar switch, and a “primary AHB” complex. It contains the 16-Kbyte L1 instruction cache, 16-Kbyte L1 data cache, 32-Kbyte ROM and 128-Kbyte RAM. |
| ATA | ATA module | Connectivity peripherals | The ATA module is an AT attachment host interface. Its main use is to interface with IDE hard disc drives and ATAPI optical disc drives. It interfaces with the ATA device over a number of ATA signals. |
| AUDMUX | Digital audio mux | Multimedia peripherals | The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (SSIs) and peripheral serial interfaces (audio codecs). The AUDMUX has two sets of interfaces: internal ports to on-chip peripherals, and external ports to off-chip audio devices. Data is routed by configuring the appropriate internal and external ports. |
| CCM | Clock control module | Clocks | This block generates all clocks for the iMX25 system. The CCM also manages the ARM926 Platform's low-power modes (wait, stop, and doze) by disabling peripheral clocks appropriately for power conservation. |
| CSPI(3) | Configurable serial peripheral interface | Connectivity peripherals | This module is a serial interface equipped with data FIFOs. Each master/slave-configurable SPI module is capable of interfacing to both serial port interface master and slave devices. The CSPI ready (SPI_RDY) and slave select (SS) control signals enable fast data communication with fewer software interrupts. |
| DRYICE | DRYICE module | Security | DRYICE provides volatile key storage for point-of-sale (POS) terminals, and a trusted time source for digital rights management (DRM) schemes. Several tamper-detect circuits are also provided to support key erasure and time invalidation in the event of tampering. Alarms and/or interrupts can also assert if tampering is detected. |
| EMI | External memory interface | Connectivity peripherals | The external memory interface (EMI) module provides access to external memory for the ARM and other masters. It is composed of four main submodules: <ul style="list-style-type: none"> • M3IF provides arbitration between multiple masters requesting access to the external memory. • Enhanced SDRAM/LPDDR memory controller (ESDCTL) interfaces to DDR2 and SDR interfaces. • NAND Flash controller (NFC) provides an interface to NAND Flash memories. • Wireless external interface memory controller (WEIM) interfaces to NOR Flash and PSRAM. |

Table 2. i.MX25 Digital and Analog Modules (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|----------------|---|----------------------------|---|
| EPIT(2) | Enhanced periodic interrupt timer | Timer peripherals | Each enhanced periodic interrupt timer (EPIT) is a 32-bit set-and-forget timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler to adjust the input clock frequency to the required time setting for the interrupts, and the counter value can be programmed on the fly. |
| ESAI | Enhanced serial audio interface | Connectivity peripherals | ESAI provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other DSPs. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. |
| eSDHC(2) | Enhanced multimedia card/secure digital host controller | Connectivity peripherals | The features of the eSDHC module, when serving as host, include the following: <ul style="list-style-type: none"> • Conforms to the SD host controller standard specification version 2.0 • Compatible with the JEDEC MMC system specification version 4.2 • Compatible with the SD memory card specification version 2.0 • Compatible with the SDIO specification version 1.2 • Designed to work with SD memory, miniSD memory, SDIO, miniSDIO, SD combo, MMC and MMC RS cards • Configurable to work in one of the following modes: <ul style="list-style-type: none"> —SD/SDIO 1-bit, 4-bit —MMC 1-bit, 4-bit, 8-bit • Full-/high-speed mode • Host clock frequency variable between 32 kHz and 52 MHz • Up to 200-Mbps data transfer for SD/SDIO cards using four parallel data lines • Up to 416-Mbps data transfer for MMC cards using eight parallel data lines |
| FEC | Fast ethernet controller | Connectivity peripherals | The Ethernet media access controller (MAC) is designed to support both 10- and 100-Mbps Ethernet networks compliant with IEEE 802.3 [®] standard. An external transceiver interface and transceiver function are required to complete the interface to the media |
| FlexCAN(2) | Controller area network module | Connectivity peripherals | The controller area network (CAN) protocol is primarily designed to be used as a vehicle serial data bus running at 1 MBps. |
| GPIO(4) | General purpose I/O modules | System control peripherals | Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O. |
| GPT(4) | General purpose timers | Timer peripherals | Each GPT is a 32-bit free-running or set-and-forget mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in set-and-forget mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock. |

Table 2. i.MX25 Digital and Analog Modules (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|-----------------------|---|----------------------------|---|
| I ² C(3) | I ² C module | Connectivity peripherals | Inter-IC Communication (I ² C) is an industry-standard, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. I ² C is suitable for applications requiring occasional communications over a short distance between many devices. The interface operates up to 100 kbps with maximum bus loading and timing. The I ² C system is a true multiple-master bus, including arbitration and collision detection that prevents data corruption if multiple devices attempt to control the bus simultaneously. This feature supports complex applications with multiprocessor control and can be used for rapid testing and alignment of end products through external connections to an assembly-line computer. |
| IIM | IC Identification Module | Security | The IIM provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, and various control signals requiring a fixed value. |
| IOMUX | I/O multiplexer | Pins | Each I/O multiplexer provides a flexible, scalable multiplexing solution: <ul style="list-style-type: none"> • Up to eight output sources multiplexed per pin • Up to four destinations for each input pin • Unselected input paths are held at constant level for reduced power consumption |
| KPP | Keypad port | Connectivity peripherals | KPP can be used for either keypad matrix scanning or general purpose I/O. |
| LCDC | LCD Controller | Multimedia peripherals | LCDC provides display data for external gray-scale or color LCD panels. LCDC is capable of supporting black-and-white, gray-scale, passive-matrix color (passive color or CSTN), and active-matrix color (active color or TFT) LCD panels. |
| MAX | ARM platform multilayer AHB crossbar switch | ARM platform | MAX concurrently supports up to five simultaneous connections between master ports and slave ports. MAX allows for concurrent transactions to occur from any master port to any slave port. |
| PWM(4) | Pulse width modulation | Connectivity peripherals | The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. The PWM uses 16-bit resolution and a 4x16 data FIFO to generate sound. |
| SDMA | Smart DMA engine | System control | The SDMA provides DMA capabilities inside the processor. It is a shared module that implements 32 DMA channels. |
| SIM(2) | Subscriber identity module interface | Connectivity peripherals | The SIMv2 is an asynchronous interface with additional features for allowing communication with smart cards conforming to the ISO/IEC 7816 specification. The SIM is designed to facilitate communication to SIM cards or pre-paid phone cards. |
| SJC | Secure JTAG interface | System control peripherals | The system JTAG controller (SJC) provides debug and test control with maximum security. |
| SLCD | Smart LCD controller | Multimedia peripherals | The SLCDC module transfers data from the display memory buffer to the external display device. |
| SPBA | Shared peripheral bus arbiter | System control | The SPBA controls access to the shared peripherals. It supports shared peripheral ownership and access rights to an owned peripheral. |

Table 2. i.MX25 Digital and Analog Modules (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|-------------------|--|--------------------------|--|
| SSI(2) | I2S/SSI/AC97 interface | Connectivity peripherals | The SSI is a full-duplex serial port that allows the processor to communicate with a variety of serial protocols, including the Freescale Semiconductor SPI standard and the inter-IC sound bus standard (I2S). The SSIs interface to the AUDMUX for flexible audio routing. |
| TSC (and ADC) | Touchscreen controller (and A/D converter) | Multimedia peripherals | The touchscreen controller and associated analog-to-digital converter (ADC) together provide a resistive touchscreen solution. The module implements simultaneous touchscreen control and auxiliary ADC operation for temperature, voltage, and other measurement functions. |
| UART(5) | UART interface | Connectivity peripherals | Each of the UART modules supports the following serial data transmit/receive protocols and configurations: <ul style="list-style-type: none"> • 7- or 8-bit data words, one or two stop bits, programmable parity (even, odd, or none) • Programmable baud rates up to 4 MHz. This is a higher maximum baud rate than the 1.875 MHz specified by the TIA/EIA-232-F standard and previous Freescale UART modules. 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA-1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE |
| USBOTG USBHOST | High-speed USB on-the-go | Connectivity peripherals | The USB module provides high-performance USB On-The-Go (OTG) and host functionality (up to 480 Mbps), compliant with the USB 2.0 specification, the OTG supplement, and the ULPI 1.0 Low Pin Count specification. The module has DMA capabilities for handling data transfer between internal buffers and system memory. An OTG HS PHY and HOST FS PHY are also integrated. |

2.1 Special Signal Considerations

Special signal considerations are listed in [Table 3](#). The package contact assignment is found in [Section 4](#), “[Package Information and Contact Assignment](#).” Signal descriptions are provided in the reference manual.

Table 3. Signal Considerations

| Signal | Description |
|----------------|---|
| BAT_VDD | Drylce backup power supply input. |
| CLK0 | Clock-out pin; renders the internal clock visible to users for debugging. The clock source is controllable through CRM registers. This pin can also be configured (via muxing) to work as a normal GPIO. |
| CLK_SEL | Used to select the ARM clock source from MPLL out or from external EXT_ARMCLK. In normal operation, CLK_SEL should be connected to GND. |
| EXT_ARMCLK | Primarily for Freescale factory use. There is no internal on-chip pull-up/down on this pin, so it must be externally connected to GND or VDD. Aside from factory use, this pin can also be configured (via muxing) to work as a normal GPIO. |
| MESH_C, MESH_D | Wire-mesh tamper detect pins that can be routed at the PCB board to detect attempted tampering of a protected wire. When security measures are implemented, MESH_C should be pulled-up to NVCC_DRYICE and triggers a tamper event when floating or when connected to MESH_D. MESH_D should be pulled-down to GND and triggers an event when floating or connected to MESH_C. These pins can be left unconnected if the Drylce security features are not being used. |

Table 3. Signal Considerations (continued)

| Signal | Description |
|-----------------------------|--|
| NVCC_DRYICE | Drylce power supply output. Source can be SoC supply or backup supply. This pin can be used to power external components (external tamper detect, wire-mesh tamper detect). |
| OSC_BYP | The 32 kHz oscillator bypass-control pin. If this signal is pulled down, then OSC32K_EXTAL and OSC32K_XTAL analog pins should be tied to the external 32.768 kHz crystal circuit. If on the other hand the signal is pulled up, then the external 32 kHz oscillator output clock must be connected to OSC32K_EXTAL analog pin, and OSC32K_XTAL can be no connect (NC). |
| OSC32K_EXTAL OSC32K_XTAL | These analog pins are connected to an external 32 kHz CLK circuit depending on the state of OSC_BYP pin (see the description of OSC_BYP under the preceding bullet). The 32 kHz reference CLK is required for normal operation. |
| POWER_FAIL | An interrupt from PMIC, which should be connected to a low-battery detection circuit. This signal is internally connected to an on-chip 100 k Ω pull-down device. If there is no low-battery detection, then users can tie this pin to GND via a pull-down resistor, or leave the signal as NC. This pin can also be configured to work as a normal GPIO. |
| REF | External ADC reference voltage (2.5 V). REF may be left floating if the internally generated 2.5 V supply is enabled. Use of an external 2.5 V reference voltage is recommended. |
| SJC_MOD | Must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 k Ω) is allowed, but the value should be much smaller than the on-chip 100-k Ω pull-up. |
| TAMPER_A, TAMPER_B | Drylce external tamper detect pins, active high. If either TAMPER_A or TAMPER_B asserted, then external tampering is detected. These pins can be left unconnected if the Drylce security features are not being used. |
| TEST_MODE | For Freescale factory use only. This signal is internally connected to an on-chip pull-down device. Users must either float this signal or tie it to GND. |
| UPLL_BYPCLK | Primarily for Freescale factory use. There is no internal on-chip pull-up/down on this pin, so it must be externally connected to GND or VDD. Aside from factory use, this pin can also be configured (via muxing) to work as a normal GPIO. |
| USBPHY1_RREF | Determines the reference current for the USB PHY1 bandgap reference. An external 10 k Ω 1% resistor to GND is required. |
| USBPHY2_DM USBPHY2_DP | The output impedance of these signals is expected at 10 Ω . It is recommended to also have on-board 33 Ω series resistors (close to the pins). |

3 Electrical Characteristics

This section provides the device-level and module-level electrical characteristics for the i.MX25.

3.1 i.MX25 Chip-Level Conditions

This section provides the chip-level electrical characteristics for the IC.

3.1.1 DC Absolute Maximum Ratings

Table 4 provides the DC absolute maximum operating conditions.

CAUTION

- Stresses beyond those listed under Table 4 may cause permanent damage to the device.
- Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- Table 4 gives stress ratings only—functional operation of the device is not implied beyond the conditions indicated in Table 5.

Table 4. DC Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Units |
|----------------------------------|---------------|------|-------------------|-------|
| Supply voltage | QV_{DD} | -0.5 | 1.52 | V |
| Supply voltage (level shift i/o) | $V_{DDIOmax}$ | -0.5 | 3.6 | V |
| ESD damage immunity: | V_{esd} | | | V |
| Human body model (HBM) | | — | 2000 ¹ | |
| Charge device model (CDM) | | — | 500 ¹ | |
| Input voltage range | $V_{I_{max}}$ | -0.5 | $NV_{DD} + 0.3$ | V |
| Storage temperature range | $T_{storage}$ | -40 | 105 | °C |

¹ ESD values will be verified during qualification.

3.1.2 DC Operating Conditions

Table 5 provides the DC recommended operating conditions.

Table 5. DC Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|--|------------------|-------------------|------|------|-------|
| Core supply voltage (at 266 MHz) | QV_{DD} | 1.15 ¹ | 1.34 | 1.52 | V |
| Core supply voltage (at 400 MHz) | QV_{DD} | 1.38 ¹ | 1.45 | 1.52 | V |
| Coin battery ² BAT_VDD | V_{DD_BAT} | 1.15 | — | 1.55 | V |
| I/O supply voltage, GPIO NFC,CSI,SDIO | NV_{DD_GPIO1} | 1.75 | — | 3.6 | V |

Table 5. DC Operating Conditions (continued)

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|--|--------------------------------|------|---------------|---------------|-------|
| I/O supply voltage, GPIO CRM,LCDC,JTAG,MISC | NV_{DD_GPIO2} | 3.0 | 3.3 | 3.6 | — |
| I/O supply voltage DDR (Mobile DDR mode) EMI1, EMI2 | NV_{DD_MDDR} | 1.75 | — | 1.95 | V |
| I/O supply voltage DDR (DDR2 mode) EMI1,EMI2 | NV_{DD_DDR2} | 1.75 | — | 1.9 | V |
| I/O supply voltage DDR (SDRAM mode) EMI1,EMI2 | NV_{DD_SDRAM} | 1.75 | — | 3.6 | V |
| Supply of USBPHY1 (HS) USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD,USBPHY1_VDDA | $V_{DD_usbphy1}$ | 3.17 | 3.3 | 3.43 | V |
| Supply of USBPHY2 (FS) USBPHY2_VDD | $V_{DD_usbphy2}$ | 3.0 | 3.3 | 3.6 | V |
| Supply of OSC24M OSC24M_VDD | V_{DD_OSC24M} | 3.0 | 3.3 | 3.6 | V |
| Supply of PLL MPLL_VDD,UPLL_VDD | V_{DD_PLL} | 1.4 | — | 1.65 | V |
| Supply of touchscreen ADC NVCC_ADC | V_{DD_tsc} | 3.0 | 3.3 | 3.6 | V |
| External reference of touchscreen ADC Ref | Vref | 2.5 | V_{DD_tsc} | V_{DD_tsc} | V |
| Fusebox program supply voltage FUSE_VDD ³ | $FUSEV_{DD}$ (program mode) | — | 3.6 | — | V |
| Supply output ⁴ NVCC_DRYICE | $V_{DD_}$ | 1.0 | — | 1.55 | V |
| Operating ambient temperature | T_A | −40 | — | 85 | °C |

¹ Values must be verified

² V_{DD_BAT} must always be powered by battery in security application. In non-security case, V_{DD_BAT} can be connected to QV_{DD} .

³ The fusebox read supply is connected to supply of the full speed USBPHY2_VDD. FUSE_VDD is only used for programming. It is recommended that FUSE_VDD be connected to ground when not being used for programming. See Table 6 for current parameters.

⁴ NVCC_DRYICE is supply output. A 0.1-μF external capacitor should be connected to it.

3.1.3 Fusebox Supply Current Parameters

Table 6 lists the fusebox supply current parameters.

Table 6. Fusebox Supply Current Parameters

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|--|----------------------|------|------|------|-------|
| eFuse program current ¹ Current to program one eFuse bit The associated VDD_FUSE supply = 3.6 V | I_{program} | 26 | 35 | 62 | mA |
| eFuse read current ² Current to read an 8-bit eFuse word | I_{read} | — | 12.5 | 15 | mA |

¹ The current I_{program} is during program time (t_{program}).

² The current I_{read} is present for approximately 50 ns of the read access to the 8-bit word.

3.1.4 Interface Frequency Limits

Table 7 provides information for interface frequency limits.

Table 7. Interface Frequency Limits

| Parameter | Min. | Typ. | Max. | Units |
|----------------------------------|------|--------|------|-------|
| JTAG: TCK Frequency of Operation | DC | 5 | 10 | MHz |
| OSC24M_XTAL Oscillator | — | 24 | — | MHz |
| OSC32K_XTAL Oscillator | — | 32.768 | — | KHz |

3.1.5 USB_PHY Current Consumption

Table 8 provides information for USB_PHY current consumption.

Table 8. USB PHY Current Consumption¹

| Parameter | Conditions | | Typ. (@Typ. Temp) | Max. (@Max. Temp) | Unit |
|---|------------|----|----------------------|----------------------|---------------|
| Analog supply USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD, USBPHY1_VDDA (3.3 V) | Full speed | Rx | 11.4 | — | mA |
| | | Tx | 22.6 | — | |
| | High speed | Rx | 21.5 | — | |
| | | Tx | 33.8 | — | |
| | Suspend | — | 0.6 | — | μA |
| Analog supply USBPHY2_VDD (3.3 V) | Full Speed | Rx | 120 | — | μA |
| | | Tx | 25 | — | mA |
| | Low Speed | Rx | 252 | — | μA |
| | | Tx | 5.5 | — | mA |
| All supplies | Suspend | | 50 | 100 | μA |

¹ Values must be verified

3.1.6 Power Modes

Table 9 describes the core, clock, and module settings for the different power modes of the processor.

Table 9. i.MX25 Power Mode Settings¹

| Core/Clock/Module | Power Mode | | | | |
|-------------------|-----------------------|----------------------------|-------------------------|------------------|------------------|
| | Doze | Wait | Stop/Sleep ² | Run (266 MHz) | Run (400 MHz) |
| ARM core | Platform clock is off | In wait-for-interrupt mode | — | Active @ 266 MHz | Active @ 400 MHz |
| Well bias | On | Off | On | Off | Off |
| MCU PLL | On | On | Off | On | On |
| USB PLL | Off | Off | Off | On | On |
| OSC24M | On | On | Off | On | On |
| OSC32K | On | On | On | On | On |
| Other modules | Off | Off | Off | On | On |

¹ Values must be verified.

² Sleep mode differs from stop mode in that the core voltage is reduced to 1 V.

Table 10 describes the current consumption for the various power supplies under the various power modes.

Table 10. i.MX25 Power Mode Current Consumption

| Power Group | Power Supplies | Voltage Setting | Current Consumption for Power Modes | | | | | |
|--------------------|--|-----------------|-------------------------------------|-------------------|--------------------------|--------------------|----------------------------|----------------------------|
| | | | Doze ¹ | Wait ¹ | Stop ¹ | Sleep ¹ | Run @ 266 MHz ¹ | Run @ 400 MHz ¹ |
| FUSE_VDD | FUSE_VDD | 1.8 V | 0.04 mA | 0.04 mA | 0.04 mA | — | — | — |
| NVCC_EMI | NVCC_EMI1 NVCC_EMI2 | 1.8 V | 10.12 mA | 10.11 mA | 0.09 mA | — | — | — |
| NVCC_CRM | NVCC_CRM | 3.3 V | 0.35 mA | 0.35 mA | 0.15 mA | — | — | — |
| NVCC_OTHER | NVCC_SDIO NVCC_CSI NVCC_NFC NVCC_JTAG NVCC_LCDC NVCC_MISC | 3.3 V | 0.4 mA | 0.4 mA | 0.04 mA | — | — | — |
| NVCC_ADC | NVCC_ADC | 3.3 V | 0.03 mA | 0.03 mA | 0.03 mA | — | — | — |
| OSC24M | OSC24M_VDD | 3.3 V | 0.6 mA | 0.6 mA | 0.04 mA | — | — | — |
| PLL_VDD | MPLL_VDD UPLL_VDD | 1.5 V | 10.5 mA | 9.75 mA | 0.08 mA | — | — | — |
| QVDD | QVDD | 1.2 V | 396 μ A | 620 μ A | 396 μ A ¹ | 222 μ A | 84 mA | 136 mA |
| USBPHY1_VDDA | USBPHY1_VDDA | 3.3 V | — | — | — | — | — | — |
| USBPHY1_VDDA_VBIAS | USBPHY1_VDDA_VBIAS | 3.3 V | — | — | — | — | — | — |
| USBPHY1_UPLL_VDD | USBPHY1_UPLL_VDD | 3.3 V | — | — | — | — | — | — |
| USBPHY2 | USBPHY2_VDD | 3.3 V | 0.16 mA | 0.16 mA | 0.16 mA | — | — | — |
| TOTAL | | — | — | — | — | — | — | — |

¹ Values must be verified.

3.2 Supply Power-Up/Power-Down Requirements and Restrictions

Any i.MX25 board design must comply with the power-up and power-down sequence guidelines given in this section to ensure reliable operation of the device. Recommended power-up and power-down sequences are given in the following subsections.

CAUTION

Deviations from the guidelines in this section may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the i.MX25 (worst-case scenario)

NOTE

For security applications, the coin battery must be connected during both power-up and power-down sequences to ensure that security keys are not unintentionally erased.

3.2.1 Power-Up Sequence

The following power-up sequence is recommended:

1. Assert power on reset (POR).
2. Turn on digital logic domain and I/O power supplies VDD_n and NVCC_x.
3. Turn on all other analog power supplies, including USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD, USBPHY1_VDDA, USBPHY2_VDD, OSC24M_VDD, MPPLL_VDD, UPLL_VDD, NVCC_ADC, and FUSEVDD (FUSEVDD is tied to GND if fuses are not being programmed). The minimum time between turning on each power supply is the time it takes for the previous supply to be stable.
4. Negate the POR signal.

NOTE

- The user is advised to connect FUSEVDD to GND except when fuses are being programmed, in order to prevent unintentional blowing of fuses.
- Other power-up sequences may be possible; however, the above sequence has been verified and is recommended.

Figure 2 shows the power-up sequence diagram. After POR_B is asserted, Core VDD and NVDD_x can be powered up. After Core VDD and NVDD_x are stable, the analog supplies can be powered up.

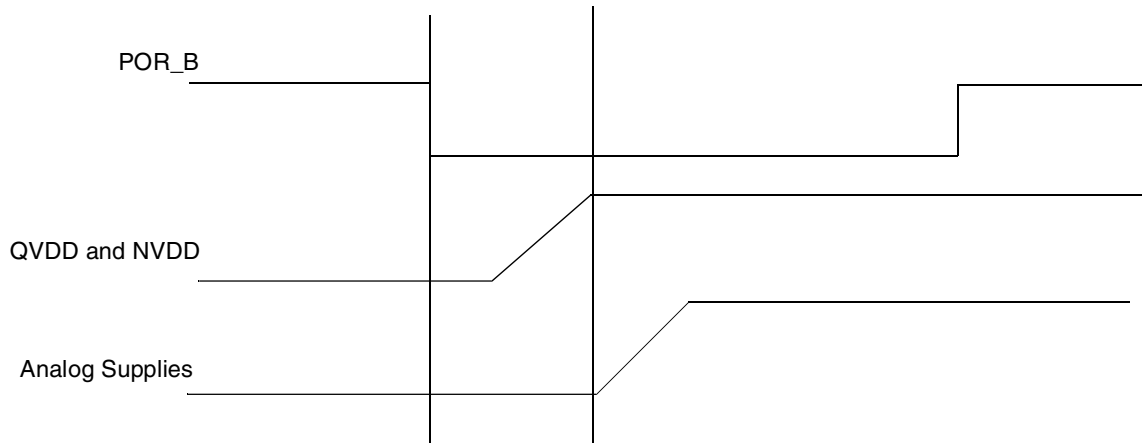


Figure 2. Power-Up Sequence Diagram

3.2.2 Power-Down Sequence

There are no special requirements for the power-down sequence. All power supplies can be shut down at the same time.

3.3 Thermal Characteristics

The thermal resistance characteristics for the device are given in [Table 11](#). These values were measured under the following conditions:

- Two-layer substrate
- Substrate solder mask thickness: 0.025 mm
- Substrate metal thicknesses: 0.016 mm
- Substrate core thickness: 0.200 mm
- Core via I.D: 0.118 mm, Core via plating 0.016 mm.
- Flag: Trace style with ground balls under the die connected to the flag
- Die Attach: 0.033 mm non-conductive die attach, $k = 0.3 \text{ W/m K}$
- Mold compound: Generic mold compound; $k = 0.9 \text{ W/m K}$

Table 11. Thermal Resistance Data

| Rating | Condition | Symbol | Value | Unit |
|---|-------------------------|--------------|-------|------|
| Junction to ambient ¹ natural convection | Single layer board (1s) | R_{eJA} | 55 | °C/W |
| Junction to ambient ¹ natural convection | Four layer board (2s2p) | R_{eJA} | 33 | °C/W |
| Junction to ambient ¹ (@200 ft/min) | Single layer board (1s) | R_{eJMA} | 46 | °C/W |
| Junction to ambient ¹ (@200 ft/min) | Four layer board (2s2p) | R_{eJMA} | 29 | °C/W |
| Junction to boards ² | — | R_{eJB} | 22 | °C/W |
| Junction to case (top) ³ | — | R_{eJCtop} | 13 | °C/W |
| Junction to package top ⁴ | Natural convection | Ψ_{JT} | 2 | °C/W |

- ¹ Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
- ² Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for this package.
- ³ Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
- ⁴ Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, this thermal characterization parameter is written as Psi-JT.

3.4 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- DDR I/O: Mobile DDR (mDDR), double data rate (DDR2), or Synchronous dynamic random access memory (SDRAM)
- General purpose I/O (GPIO)

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output. The association is shown in the “Signal Multiplexing” chapter of the reference manual.

3.4.1 DDR I/O DC Parameters

The DDR pad type is configured by the IOMUXC_SW_PAD_CTL_GRP_DDRTYPE register (see the External Signals and Pin Multiplexing chapter of the *i.MX25 Reference Manual* for details).

3.4.1.1 DDR_TYPE = 00 Standard Setting DDR I/O DC Parameters

Table 12 shows the I/O parameters for mobile DDR. These settings are suitable for mDDR and DDR2 1.8V ($\pm 5\%$) applications.

Table 12. Mobile DDR I/O DC Electrical Characteristics

| DC Electrical Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Units | Notes |
|------------------------------------|----------|---|---|------|----------------------------------|-------|-------|
| High-level output voltage | Voh | $I_{OH} = -1\text{mA}$ $I_{OH} = \text{Specified Drive}$ | OVDD – 0.08 $0.8 \times \text{OVDD}$ | — | — | V | 1 |
| Low-level output voltage | Vol | $I_{OL} = 1\text{mA}$ $I_{OL} = \text{Specified Drive}$ | — | — | 0.08 $0.2 \times \text{OVDD}$ | V | |
| High-level output current | I Ioh | Voh = $0.8 \times \text{OVDDV}$ Standard Drive High Drive Max. Drive | –3.6 –7.2 –10.8 | — | — | mA | — |
| Low-level output current | I Iol | Vol = $0.2 \times \text{OVDDV}$ Standard Drive High Drive Max. Drive | 3.6 7.2 10.8 | — | — | mA | — |
| High-level DC CMOS input voltage | VIH | — | $0.7 \times \text{OVDD}$ | OVDD | OVDD+0.3 | V | — |
| Low-level DC CMOS input voltage | VIL | — | –0.3 | 0 | $0.3 \times \text{OVDD}$ | V | |
| Differential receiver VTH+ | VTH+ | — | | — | 100 | mV | |
| Differential receiver VTH- | VTH- | — | –100 | — | — | mV | |
| Input current (no pull-up/down) | IIN | VI = 0 VI = OVDD | — | — | 110 60 | nA | 2, 3 |
| High-impedance I/O supply current | Icc-ovdd | VI = OVDD or 0 | — | — | 990 | nA | 2, 3 |
| High-impedance core supply current | Icc-vddi | VI = VDD or 0 | — | — | 1220 | nA | |

Note:

- Simulation circuit for parameters Voh and Vol for I/O cells is below
- Minimum condition: BCS model, 1.95 V, and –40 °C. Typical condition: typical model, 1.8 V, and 25 °C. Maximum condition: wcs model, 1.65 V, and 105 °C.
- Typical condition: typical model, 1.8 V, and 25 °C. Maximum condition: BCS model, 1.95 V, and 105 °C.

3.4.1.2 DDR_TYPE = 01 SDRAM I/O DC Parameters

Table 13 shows the DC I/O parameters for SDRAM.

Table 13. SDRAM DC Electrical Characteristics

| DC Electrical Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Units | Notes |
|------------------------------------|----------|--|-----------------------|------|-----------|-------|-------|
| High-level output voltage | Voh | Ioh = Specified Drive (Ioh = -4, -8, -12, -16mA) | 2.4 | — | — | V | 1 |
| Low-level output voltage | Vol | Ioh = Specified Drive (Ioh = 4, 8, 12, 16mA) | — | — | 0.4 | V | 1 |
| High-level output current | I Ioh | Standard Drive High Drive Max. Drive | -4.0 -8.0 -12.0 | — | — | mA | — |
| Low-level output current | I Iol | Standard Drive High Drive Max. Drive | 4.0 8.0 12.0 | — | — | mA | — |
| High-level DC input voltage | VIH | — | 2.0 | — | 3.6 | V | — |
| Low-level DC input voltage | VIL | — | -0.3 V | — | 0.8 | V | |
| Input current (no pull-up/down) | IIN | VI = 0 VI = OVDD | — | — | 150 80 | nA | 2, 3 |
| High-impedance I/O supply current | Icc-ovdd | VI = OVDD or 0 | — | — | 1180 | nA | 2, 3 |
| High-impedance core supply current | Icc-vddi | VI = VDD or 0 | — | — | 1220 | nA | |

Note:

- Simulation circuit for parameters Voh and Vol for I/O cells is below
- Minimum condition: bcs model, OVDD = 3.6 V, and -40 °C. Typical condition: typical model, OVDD = 3.3 V, and 25 °C. Maximum condition: wcs model, OVDD = 3.0 V, and 105 °C.
- Typical condition: typical model, OVDD = 3.3 V, and 25 °C. Maximum condition: bcs model, OVDD = 3.6 V, and 105 °C.

3.4.1.3 DDR_TYPE = 10 Max Setting DDR I/O DC Parameters

Table 14 shows the I/O parameters for DDR2 (SSTL_18).

Table 14. DDR2 (SSTL_18) I/O DC Electrical Characteristics

| DC Electrical Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Units | Notes |
|-------------------------------|---------|-----------------|----------------|------|----------------|-------|-------|
| High-level output voltage | Voh | — | OVDD - 0.28 | — | — | V | — |
| Low-level output voltage | Vol | — | — | — | 0.28 | V | |
| Output min. source current | Iloh | — | -13.4 | — | — | mA | 1 |
| Output min. sink current | Iol | — | 13.4 | — | — | mA | 2 |
| DC input logic high | VIH(dc) | — | OVDD/2 + 0.125 | — | OVDD + 0.3 | V | — |
| DC input logic low | VIL(dc) | — | -0.3 V | — | OVDD/2 - 0.125 | V | — |

Table 14. DDR2 (SSTL_18) I/O DC Electrical Characteristics (continued)

| DC Electrical Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Units | Notes |
|--|----------|---------------------|---------------|--------|---------------|-------|-------|
| DC input signal voltage(for differential signal) | Vin(dc) | — | -0.3 | — | OVDD + 0.3 | V | 3 |
| DC differential input voltage | Vid(dc) | — | 0.25 | — | OVDD+0.6 | V | 4 |
| Termination voltage | Vtt | — | OVDD/2 – 0.04 | OVDD/2 | OVDD/2 + 0.04 | | 5 |
| Input current (no pull-up/down) | IIN | VI = 0 VI = OVDD | — | — | 110 60 | nA | 9 |
| High-impedance I/O supply current | Icc-ovdd | VI = OVDD or 0 | — | — | 980 | nA | 9 |
| High-impedance core supply current | Icc-vddi | VI = VDD or 0 | — | — | 1210 | nA | |

Note:

- OVDD = 1.7 V; V_{out} = 1.42 V. (V_{out}-OVDD)/IOH must be less than 21 W for values of V_{out} between OVDD and OVDD-0.28 V.
- OVDD = 1.7 V; V_{out} = 280 mV. V_{out}/IOL must be less than 21 W for values of V_{out} between 0 V and 280 mV. Simulation circuit for parameters V_{oh} and V_{ol} for I/O cells is below
- Vin(dc) specifies the allowable DC excursion of each differential input
- Vid(dc) specifies the input differential voltage required for switching. The minimum value is equal to Vih(dc) - Vil(dc).
- Vtt is expected to track OVDD/2.
- Minimum condition: BCS model, 1.95 V, and -40 °C. Typical condition: typical model, 1.8 V, and 25 °C. Maximum condition: wcs model, 1.65 V, and 105 °C.
- Typical condition: typical model, 1.8 V, and 25 °C. Maximum condition: BCS model, 1.95 V, and 105 °C.
- The JEDEC SSTL_18 specification (JESD8-15a) for a SSTL interface for class II operation supersedes any specification in this document.

3.4.2 GPIO I/O DC Parameters

Table 15 shows the I/O parameters for GPIO.

Table 15. GPIO DC Electrical Characteristics

| DC Electrical Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Units | Notes |
|---|----------|--|---------------------------|------|--------------------|-------|-------|
| High-level output voltage | Voh | Ioh=-1mA Ioh = Specified Drive | OVDD – 0.15 0.8 × OVDD | — | — | V | 1 |
| Low-level output voltage | Vol | Iol=1mA Iol=Specified Drive | — | — | 0.15 0.2 × OVDD | V | 1 |
| High-level output current for slow mode | I Ioh | Voh=0.8 × OVDD Standard Drive High Drive Max. Drive | -2.0 -4.0 -8.0 | — | — | mA | — |
| High-level output current for fast mode | I Ioh | Voh=0.8 × OVDD Standard Drive High Drive Max. Drive | -4.0 -6.0 -8.0 | — | — | mA | — |

Table 15. GPIO DC Electrical Characteristics (continued)

| DC Electrical Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Units | Notes |
|--|------------------|--|-------------------------------|------|--------------------------------|-------|-------|
| Low-level output current for slow mode | I | Voh=0.2 × OVDD | 2.0 | — | — | mA | — |
| | I _{ol} | Standard Drive | 4.0 | | | | |
| | | High Drive | 8.0 | | | | |
| Low-level output current for fast mode | I | Voh=0.2 × OVDD | 4.0 | — | — | mA | — |
| | I _{ol} | Standard Drive | 6.0 | | | | |
| | | High Drive | 8.0 | | | | |
| High-level DC input voltage | V _{IH} | — | 0.7 × OVDD | — | OVDD | V | — |
| Low-level DC input voltage | V _{IL} | — | −0.3 V | — | 0.3 × OVDD | V | |
| Input hysteresis | V _{HYS} | OVDD = 3.3 V OVDD = 1.8V | 370 290 | — | 420 320 | mV | — |
| Schmitt trigger V _{T+} | V _{T+} | — | 0.5 × OVDD | — | — | V | 2 |
| Schmitt trigger V _{T−} | V _{T−} | — | — | — | 0.5 × OVDD | V | |
| Pull-up resistor (22 kΩ PU) | R _{pu} | V _i =0 | 18.5 | 22 | 25.6 | KΩ | 3 |
| Pull-up resistor (47 kΩ PU) | R _{pu} | V _i =0 | 41 | 47 | 55 | KΩ | |
| Pull-up resistor (100 kΩ PU) | R _{pu} | V _i =0 | 85 | 100 | 120 | KΩ | |
| Pull-down resistor (100 kΩ PD) | R _{pd} | V _i = OVDD | 85 | 100 | 120 | KΩ | |
| Input current (no pull-up/down) | I _{IN} | V _I = 0, OVDD = 3.3 V V _I = OVDD = 3.3 V V _I = 0, OVDD = 1.8 V V _I = OVDD = 1.8 V | — | — | 100 60 77 50 | nA | 4 |
| Input current (22 kΩ PU) | I _{IN} | V _I = 0, OVDD = 3.3 V V _I = OVDD = 3.3 V V _I = 0, OVDD = 1.8 V V _I = OVDD = 1.8 V | 117 0.0001 64 0.0001 | — | 184 0.0001 104 0.0001 | μA | |

Table 15. GPIO DC Electrical Characteristics (continued)

| DC Electrical Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Units | Notes |
|------------------------------------|----------|--|------------------------------|------|------------------------------|-------|-------|
| Input current (47 kΩ PU) | IIN | VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V | 54 0.0001 30 0.0001 | — | 88 0.0001 49 0.0001 | μA | 4 |
| Input current (100 kΩ PU) | IIN | VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V | 25 0.0001 14 0.0001 | — | 42 0.0001 23 0.0001 | μA | |
| Input current (100 kΩ PD) | IIN | VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V | 25 0.0001 14 0.0001 | — | 42 0.001 23 0.0001 | μA | |
| High-impedance I/O supply current | Icc-ovdd | VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V | — | — | 688 688 560 560 | nA | 4 |
| High-impedance core supply current | Icc-vddi | VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V | — | — | 490 490 410 410 | nA | |

1. Simulation circuit for parameters Voh and Vol for I/O cells is below
2. Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.
3. Minimum condition: bcs model, OVDD = 3.6 V / 1.95 V and -40 °C. Typical condition: typical model, OVDD = 3.3 V / 1.8 V, and 25 °C. Maximum condition: wcs model, OVDD = 3.0 V, and 105 °C.
4. Typical condition: typical model, OVDD=3.3 V / 1.8 V, and 25 °C. Maximum condition: bcs model, OVDD=3.6 V / 1.95 V, and 105 °C.

3.5 AC Electrical Characteristics

This section provides the AC parameters for slow and fast I/O.

Figure 3 shows the load circuit for output. Figure 4 through Figure 6 show the output transition time and propagation waveforms.

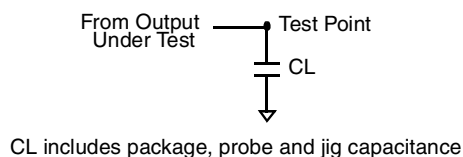


Figure 3. Load Circuit for Output

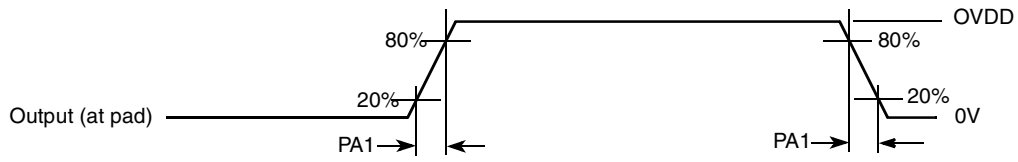


Figure 4. Output Pad Transition Time Waveform

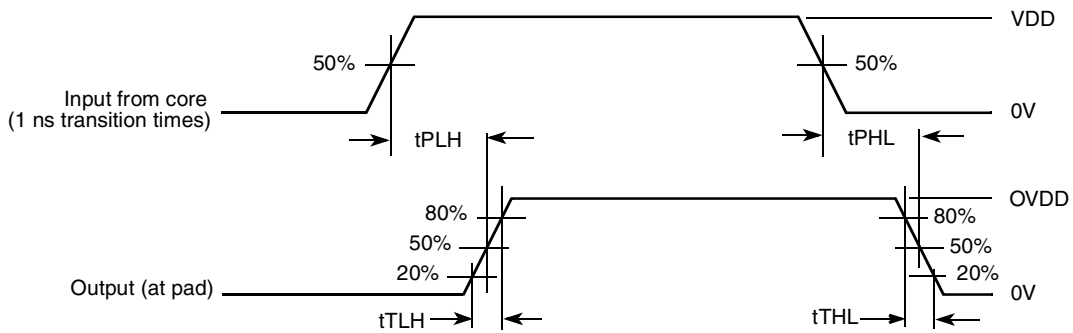


Figure 5. Output Pad Propagation and Transition Time Waveform

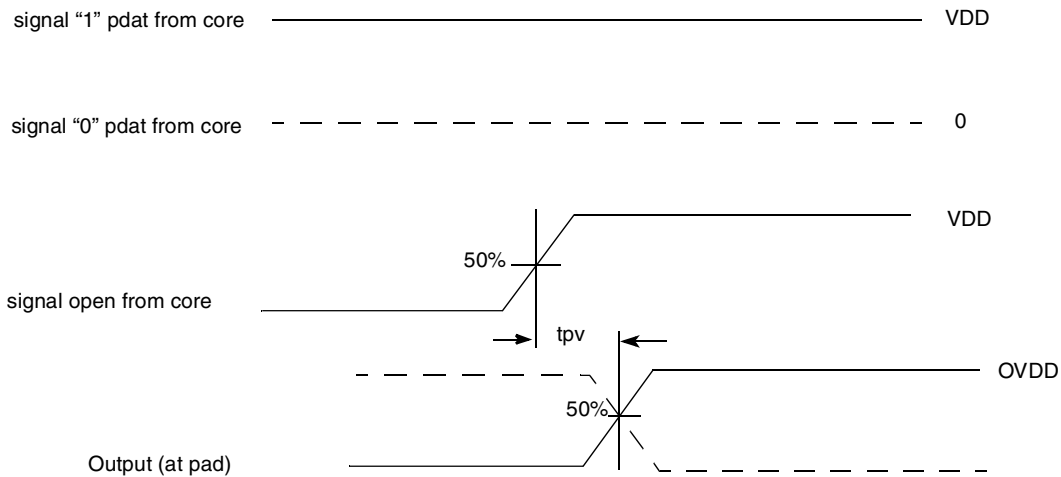


Figure 6. Output Enable to Output Valid

3.5.1 Slow I/O AC Parameters

Table 16 shows the slow I/O AC parameters.

Table 16. Slow I/O AC Parameters

| Parameter | Symbol | Test Voltage | Test Capacitance | Min. Rise/Fall | Typ. Rise/Fall | Max. Rise/Fall | Units | Notes |
|--|--------|--------------|------------------|----------------|----------------|----------------|-------|-------|
| Duty cycle | Fduty | — | — | 40 | — | 60 | % | — |
| Output pad transition times (max. drive) | tpr | 3.0–3.6 V | 25 pF | 0.95/0.84 | 1.36/1.11 | 2.06/1.60 | ns | 1 |
| | | 3.0–3.6 V | 50 pF | 1.58/1.37 | 2.19/1.77 | 3.20/2.47 | | |
| | | 1.65–1.95 V | 25 pF | 2.70/2.50 | 1.80/1.40 | 3.01/2.37 | | |
| | | 1.65–1.95 V | 50 pF | 3.40/3.20 | 2.80/2.14 | 4.63/3.38 | | |
| Output pad transition times (high drive) | tpr | 3.0–3.6 V | 25 pF | 1.60/1.39 | 2.23/1.79 | 3.26/2.50 | ns | 1 |
| | | 3.0–3.6 V | 50 pF | 2.94/2.51 | 4.05/3.17 | 5.72/4.27 | | |
| | | 1.65–1.95 V | 25 pF | 1.85/1.48 | 2.90/2.17 | 4.75/3.43 | | |
| | | 1.65–1.95 V | 50 pF | 2.93/2.37 | 4.56/3.40 | 7.33/5.26 | | |
| Output pad transition times (standard drive) | tpr | 3.0–3.6 V | 25 pF | 3.07/2.62 | 4.22/3.30 | 6.03/4.48 | ns | 1 |
| | | 3.0–3.6 V | 50 pF | 5.82/4.95 | 7.94/6.19 | 11.28/8.28 | | |
| | | 1.65–1.95 V | 25 pF | 3.04/2.47 | 4.73/3.50 | 3.01/2.36 | | |
| | | 1.65–1.95 V | 50 pF | 5.37/4.40 | 7.70/8.10 | 4.63/3.38 | | |
| Output pad propagation delay (max. drive), 50%–50% | tpo | 3.0–3.6 V | 25 pF | 1.92/2.1 | 2.96/2.96 | 4.47/4.38 | ns | 1 |
| | | 3.0–3.6 V | 50 pF | 2.44/2.53 | 3.7/3.64 | 5.54/5.31 | | |
| | | 1.65–1.95 V | 25 pF | 2.05/2.27 | 3.32/3.67 | 5.27/5.85 | | |
| | | 1.65–1.95 V | 50 pF | 2.71/2.84 | 4.39/4.51 | 7.00/7.15 | | |
| Output pad propagation delay (high drive), 50%–50% | tpo | 3.0–3.6 V | 25 pF | 2.35/2.49 | 3.58/3.61 | 5.35/5.24 | ns | 1 |
| | | 3.0–3.6 V | 50 pF | 3.31/3.43 | 4.9/4.786 | 7.19/6.8 | | |
| | | 1.65–1.95 V | 25 pF | 2.58/2.69 | 4.17/4.27 | 6.64/6.74 | | |
| | | 1.65–1.95 V | 50 pF | 3.62/3.60 | 5.86/5.61 | 9.34/8.76 | | |
| Output pad propagation delay (standard drive), 50%–50% | tpo | 3.0–3.6 V | 25 pF | 3.39/3.51 | 5.03/4.89 | 7.39/6.95 | ns | 1 |
| | | 3.0–3.6 V | 50 pF | 5.28/5.35 | 7.6/7.14 | 10.97/9.45 | | |
| | | 1.65–1.95 V | 25 pF | 3.71/3.68 | 6.03/5.75 | 9.64/8.97 | | |
| | | 1.65–1.95 V | 50 pF | 5.52/5.32 | 8.80/7.96 | 13.9/11.3 | | |
| Output pad propagation delay (max. drive), 40%–60% | tpo | 3.0–3.6 V | 25 pF | 1.942/2.04 | 2.923/2.95 | 4.33/4.3 | ns | 1 |
| | | 3.0–3.6 V | 50 pF | 2.378/2.48 | 3.541/3.53 | 5.29/5.09 | | |
| | | 1.65–1.95 V | 25 pF | 2.03/2.28 | 3.19/3.59 | 4.97/5.64 | | |
| | | 1.65–1.95 V | 50 pF | 2.59/2.73 | 4.10/4.33 | 6.43/6.77 | | |
| Output pad propagation delay (high drive), 40%–60% | tpo | 3.0–3.6 V | 25 pF | 2.29/2.44 | 3.42/3.49 | 5.05/5.02 | ns | 1 |
| | | 3.0–3.6 V | 50 pF | 3.05/3.20 | 4.46/4.45 | 6.53/6.3 | | |
| | | 1.65–1.95 V | 25 pF | 2.45/2.62 | 3.86/4.07 | 6.02/6.35 | | |
| | | 1.65–1.95 V | 50 pF | 3.36/3.39 | 5.34/5.22 | 8.40/8.08 | | |
| Output pad propagation delay (standard drive), 40%–60% | tpo | 3.0–3.6 V | 25 pF | 3.12/3.26 | 4.58/4.53 | 6.69/6.42 | ns | 1 |
| | | 3.0–3.6 V | 50 pF | 4.60/4.73 | 6.61/6.32 | 9.5/8.32 | | |
| | | 1.65–1.95 V | 25 pF | 3.43/3.46 | 5.48/5.34 | 8.65/8.26 | | |
| | | 1.65–1.95 V | 50 pF | 4.89/4.79 | 7.75/7.16 | 12.2/9.97 | | |

Table 16. Slow I/O AC Parameters (continued)

| Parameter | Symbol | Test Voltage | Test Capacitance | Min. Rise/Fall | Typ. Rise/Fall | Max. Rise/Fall | Units | Notes |
|---|--------|--------------|------------------|----------------|----------------|----------------|-------|-------|
| Output enable to output valid delay (max. drive), 50%–50% | tpv | 3.0–3.6 V | 25 pF | 2.13/2.01 | 3.3/3.045 | 5.072/4.609 | ns | 1 |
| | | 3.0–3.6 V | 50 pF | 2.65/2.46 | 4.038/3.639 | 6.142/5.423 | | |
| | | 1.65–1.95 V | 25 pF | 2.31/2.45 | 3.76/4.00 | 6.11/6.47 | | |
| | | 1.65–1.95 V | 50 pF | 2.95/3.01 | 4.81/4.82 | 7.81/7.73 | | |
| Output enable to output valid delay (high drive), 50%–50% | tpv | 3.0–3.6 V | 25 pF | 2.56/2.43 | 3.91/3.604 | 5.937/5.36 | | |
| | | 3.0–3.6 V | 50 pF | 3.55/3.21 | 5.21/4.598 | 7.776/6.694 | | |
| | | 1.65–1.95 V | 25 pF | 2.85/2.90 | 4.65/4.64 | 7.58/7.44 | | |
| | | 1.65–1.95 V | 50 pF | 3.87/3.78 | 6.31/5.95 | 10.3/9.43 | | |
| Output enable to output valid delay (standard drive), 50%–50% | tpv | 3.0–3.6 V | 25 pF | 3.60/3.28 | 5.35/4.70 | 7.97/6.836 | | |
| | | 3.0–3.6 V | 50 pF | 5.50/4.81 | 7.93/6.603 | 11.58/9.338 | | |
| | | 1.65–1.95 V | 25 pF | 4.04/3.94 | 6.65/6.21 | 10.9/9.22 | | |
| | | 1.65–1.95 V | 50 pF | 5.85/5.56 | 9.47/8.49 | 15.5/13.3 | | |
| Output enable to output valid delay (max. drive), 40%–60% | tpv | 3.0–3.6 V | 25 pF | 2.152/1.7 | 3.25/2.68 | 4.93/4.162 | ns | 1 |
| | | 3.0–3.6 V | 50 pF | 2.6/2.07 | 3.88/3.17 | 5.842/4.846 | | |
| | | 1.65–1.95 V | 25 pF | 2.28/2.46 | 3.62/3.92 | 5.77/6.24 | | |
| | | 1.65–1.95 V | 50 pF | 2.83/2.93 | 4.50/4.62 | 7.20/7.32 | | |
| Output enable to output valid delay (high drive), 40%–60% | tpv | 3.0–3.6 V | 25 pF | 2.497/2.036 | 3.75/3.135 | 5.633/4.782 | | |
| | | 3.0–3.6 V | 50 pF | 3.254/2.647 | 4.8/3.9 | 7.117/5.84 | | |
| | | 1.65–1.95 V | 25 pF | 2.71/2.81 | 4.31/4.23 | 6.89/7.01 | | |
| | | 1.65–1.95 V | 50 pF | 3.59/3.56 | 5.75/5.54 | 9.23/8.71 | | |
| Output enable to output valid delay (standard drive), 40%–60% | tpv | 3.0–3.6 V | 25 pF | 3.326/2.7 | 4.9/3.9 | 7.269/5.95 | | |
| | | 3.0–3.6 V | 50 pF | 4.81/3.85 | 6.9/5.4 | 10.12/7.86 | | |
| | | 1.65–1.95 V | 25 pF | 3.73/3.69 | 6.04/5.77 | 9.81/9.11 | | |
| | | 1.65–1.95 V | 50 pF | 5.16/4.99 | 8.28/7.61 | 13.4/11.8 | | |
| Output pad slew rate (max. drive) | tps | 3.0–3.6 V | 25 pF | 0.79/1.12 | 1.30/1.77 | 2.02/2.58 | V/ns | 2 |
| | | 3.0–3.6 V | 50 pF | 0.49/0.73 | 0.84/1.23 | 1.19/1.58 | | |
| | | 1.65–1.95 V | 25 pF | 0.30/0.42 | 0.54/0.73 | 0.91/1.20 | | |
| | | 1.65–1.95 V | 50 pF | 0.20/0.29 | 0.35/0.50 | 0.60/0.80 | | |
| Output pad slew rate (high drive) | tps | 3.0–3.6 V | 25 pF | 0.48/0.72 | 0.76/1.10 | 1.17/1.56 | | |
| | | 3.0–3.6 V | 50 pF | 0.27/0.42 | 0.41/0.62 | 0.63/0.86 | | |
| | | 1.65–1.95 V | 25 pF | 0.19/0.28 | 0.34/0.49 | 0.58/0.79 | | |
| | | 1.65–1.95 V | 50 pF | 0.12/0.18 | 0.34/0.49 | 0.36/0.49 | | |
| Output pad slew rate (standard drive) | tps | 3.0–3.6 V | 25 pF | 0.25/0.40 | 0.40/0.59 | 0.60/0.83 | | |
| | | 3.0–3.6 V | 50 pF | 0.14/0.21 | 0.21/0.32 | 0.32/0.44 | | |
| | | 1.65–1.95 V | 25 pF | 0.12/0.18 | 0.20/0.30 | 0.34/0.47 | | |
| | | 1.65–1.95 V | 50 pF | 0.07/0.11 | 0.11/0.17 | 0.20/0.27 | | |

Table 16. Slow I/O AC Parameters (continued)

| Parameter | Symbol | Test Voltage | Test Capacitance | Min. Rise/Fall | Typ. Rise/Fall | Max. Rise/Fall | Units | Notes |
|---|--------|--------------|------------------|------------------------|-----------------------|------------------------|-----------|-------|
| Output pad dl/dt (max. drive) | tdit | 3.0–3.6 V | 25 pF | 15 | 36 | 76 | mA /ns | 3 |
| | | 3.0–3.6 V | 50 pF | 16 | 38 | 80 | | |
| | | 1.65–1.95 V | 25 pF | 7 | 21 | 56 | | |
| | | 1.65–1.95 V | 50 pF | 7 | 22 | 58 | | |
| Output pad dl/dt (high drive) | tdit | 3.0–3.6 V | 25 pF | 8 | 20 | 45 | | |
| | | 3.0–3.6 V | 50 pF | 9 | 21 | 47 | | |
| | | 1.65–1.95 V | 25 pF | 5 | 14 | 38 | | |
| | | 1.65–1.95 V | 50 pF | 5 | 15 | 40 | | |
| Output pad dl/dt (standard drive) | tdit | 3.0–3.6 V | 25 pF | 4 | 10 | 22 | | |
| | | 3.0–3.6 V | 50 pF | 4 | 10 | 23 | | |
| | | 1.65–1.95 V | 25 pF | 2 | 7 | 18 | | |
| | | 1.65–1.95 V | 50 pF | 2 | 7 | 19 | | |
| Input pad propagation delay without hysteresis, 50%–50% | tpi | — | 1.6 pF | 0.82/0.47 0.74/1 | 1.1/0.76 1.1/1.5 | 1.6/1.04 1.75/2.16 | ns | 4 |
| Input pad propagation delay with hysteresis, 50%–50% | tpi | — | 1.6 pF | 1.1/1.3 1.75/1.63 | 1.43/1.6 2.67/2.22 | 2/2 2.92/3 | | |
| Input pad propagation delay without hysteresis, 40%–60% | tpi | — | 1.6 pF | 1.62/1.28 1.82/1.55 | 1.9/1.56 2.28/1.87 | 2.38/1.82 2.95/2.54 | | |
| Input pad propagation delay with hysteresis, 40%–60% | tpi | — | 1.6 pF | 1.88/2.1 2.4/2.6 | 2.2/2.4 3/3.07 | 2.7/2.75 3.77/3.71 | | |
| Input pad transition times without hysteresis | trfi | — | 1.6 pF | 0.16/0.12 | 0.23/0.18 | 0.33/0.29 | | |
| Input pad transition times with hysteresis | trfi | — | 1.6 pF | 0.16/0.13 | 0.22/0.18 | 0.33/0.29 | | |
| Maximum input transition times | trm | — | — | — | — | 25 | | |

Note:

1. Maximum condition for tpr, tpo, and tpv: wcs model, 1.1 V, I/O 3.0 V (3.0–3.6 V range) or 1.65 V (1.65–1.95 V range), and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 3.6 V (3.0–3.6 V range) or 1.95 V (1.65–1.95 V range), and –40 °C. Input transition time from core is 1 ns (20%–80%).
2. Minimum condition for tps: wcs model, 1.1 V, I/O 3.0 V (3.0–3.6 V range) or 1.65 V (1.65–1.95 V range), and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.
3. Maximum condition for tdit: bcs model, 1.3 V, I/O 3.6 V (3.0–3.6 V range) or 1.95 V (1.65–1.95 V range), and –40 °C.
4. Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 3.0 V (3.0–3.6 V range) or 1.65 V (1.65–1.95 V range), and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 3.6 V or 1.95 V (1.65–1.95 V range), and –40 °C. Input transition time from pad is 5 ns (20%–80%).
5. Hysteresis mode is recommended for input with transition time greater than 25 ns.

3.5.2 Fast I/O AC Parameters

Table 17 shows the fast I/O AC parameters for OVDD = 1.65–1.95 V.

Table 17. Fast I/O AC Parameters for OVDD = 1.65–1.95 V

| Parameter | Symbol | Test Condition | Min. Rise/Fall | Typ. | Max. Rise/Fall | Units | Notes |
|---|--------|----------------|------------------------|------------------------|------------------------|-------|-------|
| Duty cycle | Fduty | — | 40 | — | 60 | % | — |
| Output pad transition times (max. drive) | tpr | 25 pF 50 pF | 0.88/0.77 1.45/1.24 | 1.36/1.10 2.20/1.80 | 2.10/1.70 3.50/2.70 | ns | 1 |
| Output pad transition times (high drive) | tpr | 25 pF 50 pF | 1.10/0.92 1.84/1.54 | 1.65/1.33 2.80/2.20 | 2.64/2.10 4.40/3.30 | ns | |
| Output pad transition times (standard drive) | tpr | 25 pF 50 pF | 1.60/1.35 2.74/2.26 | 2.47/1.95 4.20/3.20 | 3.99/3.10 6.56/4.86 | ns | |
| Output pad propagation delay (max. drive), 50%–50% | tpo | 25 pF 50 pF | 1.64/1.53 2.15/2.01 | 2.68/2.41 3.47/3.08 | 4.25/3.74 5.50/4.77 | ns | 1 |
| Output pad propagation delay (high drive), 50%–50% | tpo | 25 pF 50 pF | 1.82/1.71 2.46/2.29 | 2.98/2.66 3.96/3.49 | 4.74/4.13 6.27/5.37 | ns | |
| Output pad propagation delay (standard drive), 50%–50% | tpo | 25 pF 50 pF | 2.24/2.06 3.17/2.92 | 3.63/3.15 5.09/4.41 | 5.73/4.84 8.06/6.75 | ns | |
| Output pad propagation delay (max. drive), 40%–60% | tpo | 25 pF 50 pF | 1.67/1.58 2.09/1.98 | 2.63/2.38 3.30/2.97 | 4.06/3.63 5.14/4.51 | ns | 1 |
| Output pad propagation delay (high drive), 40%–60% | tpo | 25 pF 50 pF | 1.94/1.73 2.34/2.22 | 2.89/2.61 3.69/3.30 | 4.49/3.97 5.76/5.01 | ns | |
| Output pad propagation delay (standard drive), 40%–60% | tpo | 25 pF 50 pF | 2.15/1.99 2.94/2.74 | 3.39/2.99 4.65/4.07 | 5.28/4.53 7.28/6.13 | ns | |
| Output enable to output valid delay (max. drive), 50%–50% | tpv | 25 pF 50 pF | 1.87/1.70 2.36/2.16 | 3.06/2.71 3.83/3.37 | 4.97/4.30 6.18/5.30 | ns | 1 |
| Output enable to output valid delay (high drive), 50%–50% | tpv | 25 pF 50 pF | 2.05/1.88 2.68/2.45 | 3.67/2.98 4.32/3.78 | 5.46/4.72 6.98/5.92 | ns | |
| Output enable to output valid delay (standard drive), 50%–50% | tpv | 25 pF 50 pF | 2.49/2.25 3.40/3.08 | 4.06/3.50 5.50/4.73 | 6.57/5.49 8.88/7.37 | ns | |
| Output enable to output valid delay (max. drive), 40%–60% | tpv | 25 pF 50 pF | 1.90/1.74 2.30/2.13 | 3.00/2.69 3.65/3.24 | 4.76/4.18 5.79/5.02 | ns | 1 |
| Output enable to output valid delay (high drive), 40%–60% | tpv | 25 pF 50 pF | 2.06/1.90 2.56/2.37 | 3.28/2.33 4.04/3.59 | 5.21/4.54 6.43/5.54 | ns | |
| Output enable to output valid delay (standard drive), 40%–60% | tpv | 25 pF 50 pF | 2.39/2.18 3.16/2.89 | 3.80/3.18 5.03/4.37 | 6.05/5.14 8.02/6.72 | ns | |
| Output pad slew rate (max. drive) | tps | 25 pF 50 pF | 0.40/0.57 0.25/0.36 | 0.72/0.97 0.43/0.61 | 1.2/1.5 0.72/0.95 | V/ns | 2 |
| Output pad slew rate (high drive) | tps | 25 pF 50 pF | 0.38/0.48 0.20/0.30 | 0.59/0.81 0.34/0.50 | 0.98/1.27 0.56/0.72 | V/ns | |
| Output pad slew rate (standard drive) | tps | 25 pF 50 pF | 0.23/0.32 0.13/0.20 | 0.40/0.55 0.23/0.34 | 0.66/0.87 0.38/0.52 | V/ns | |

Table 17. Fast I/O AC Parameters for OVDD = 1.65–1.95 V (continued)

| Parameter | Symbol | Test Condition | Min. Rise/Fall | Typ. | Max. Rise/Fall | Units | Notes |
|---|--------|----------------|----------------|-----------|----------------|-------|-------|
| Output pad dl/dt (max. drive) | tdit | 25 pF 50 pF | 7 7 | 43 46 | 112 118 | mA/ns | 3 |
| Output pad dl/dt (high drive) | tdit | 25 pF 50 pF | 11 12 | 31 33 | 81 85 | mA/ns | |
| Output pad dl/dt (standard drive) | tdit | 25 pF 50 pF | 9 10 | 27 28 | 71 74 | mA/ns | |
| Input pad propagation delay without hysteresis, 50%–50% | tpi | 1.6 pF | 0.74/1 | 1.1/1.5 | 1.75/2.16 | ns | 4 |
| Input pad propagation delay with hysteresis, 50%–50% | tpi | 1.6 pF | 1.75/1.63 | 2.67/2.22 | 2.92/3 | ns | |
| Input pad propagation delay without hysteresis, 40%–60% | tpi | 1.6 pF | 1.82/1.55 | 2.28/1.87 | 2.95/2.54 | ns | |
| Input pad propagation delay with hysteresis, 40%–60% | tpi | 1.6 pF | 2.4/2.6 | 3/3.07 | 3.77/3.71 | ns | |
| Input pad transition times without hysteresis | trfi | 1.6 pF | 0.16/0.12 | 0.30/0.18 | 0.33/0.29 | ns | |
| Input pad transition times with hysteresis | trfi | 1.6 pF | 0.16/0.13 | 0.30/0.18 | 0.33/0.29 | ns | |
| Maximum input transition times | trm | — | — | — | 25 | ns | |

Note:

1. Maximum condition for tpr, tpo, and tpv: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 1.95 V, and –40 °C. Input transition time from core is 1 ns (20%–80%).
2. Minimum condition for tps: wcs model, 1.1 V, I/O 1.65 V and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.
3. Maximum condition for tdit: bcs model, 1.3 V, I/O 1.95 V and –40 °C.
4. Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 1.65 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).
5. Hysteresis mode is recommended for input with transition time greater than 25 ns.

Table 18 shows the fast I/O AC parameters for OVDD = 3.0–3.6 V.

Table 18. Fast I/O AC Parameters for OVDD = 3.0–3.6 V

| Parameter | Symbol | Test Condition | Min. Rise/Fall | Typ. | Max. Rise/Fall | Units | Notes |
|---|--------|----------------|------------------------|------------------------|------------------------|-------|-------|
| Duty Cycle | Fduty | | 40 | | 60 | % | |
| Output Pad Transition Times (Max Drive) | tpr | 25 pF 50 pF | 0.80/0.70 1.40/1.60 | 1.12/2.51 1.60/2.39 | 1.64/1.32 2.84/2.10 | ns | 1 |
| Output Pad Transition Times (High Drive) | tpr | 25 pF 50 pF | 1.00/0.90 1.95/1.66 | 1.43/1.16 2.66/2.09 | 2.05/1.60 3.70/2.80 | ns | |
| Output Pad Transition Times (Standard Drive) | tpr | 25 pF 50 pF | 1.50/1.30 2.90/2.50 | 2.09/1.67 3.40/3.09 | 3.00/2.30 5.56/4.12 | ns | |
| Output Pad Propagation Delay (Max Drive), 50%–50% | tpo | 25 pF 50 pF | 1.20/1.28 1.67/1.75 | 1.74/1.73 2.39/2.32 | 2.67/2.52 3.58/3.33 | ns | 1 |
| Output Pad Propagation Delay (High Drive), 50%–50% | tpo | 25 pF 50 pF | 1.35/1.42 1.98/2.04 | 1.95/1.91 2.81/2.68 | 2.96/2.76 4.16/3.78 | ns | |
| Output Pad Propagation Delay (Standard Drive), 50%–50% | tpo | 25 pF 50 pF | 1.77/1.85 2.70/2.78 | 2.54/2.48 3.82/3.62 | 3.80/3.60 5.62/5.10 | ns | |
| Output Pad Propagation Delay (Max Drive), 40%–60% | tpo | 25 pF 50 pF | 1.37/1.50 1.74/1.88 | 1.94/2.05 2.46/2.55 | 2.95/3.07 3.71/3.75 | ns | 1 |
| Output Pad Propagation Delay (High Drive), 40%–60% | tpo | 25 pF 50 pF | 1.48/1.61 1.98/2.10 | 2.11/2.19 2.78/2.81 | 3.19/3.26 4.14/4.09 | ns | |
| Output Pad Propagation Delay (Standard Drive), 40%–60% | tpo | 25 pF 50 pF | 1.84/1.97 2.58/2.71 | 2.61/2.67 3.62/3.58 | 3.95/3.95 5.36/5.15 | ns | |
| Output Enable to Output Valid Delay (Max Drive), 50%–50% | tpv | 25 pF 50 pF | 1.34/1.32 1.81/1.79 | 1.91/1.81 2.56/2.40 | 2.92/2.67 3.83/3.47 | ns | 1 |
| Output Enable to Output Valid Delay (High Drive), 50%–50% | tpv | 25 pF 50 pF | 1.48/1.47 2.12/2.1 | 2.12/2.00 2.98/2.76 | 3.21/2.92 4.41/3.94 | ns | |
| Output Enable to Output Valid Delay (Standard Drive), 50%–50% | tpv | 25 pF 50 pF | 1.90/1.90 2.85/2.83 | 2.70/2.60 4.00/3.70 | 4.07/3.74 5.86/5.24 | ns | |
| Output Enable to Output Valid Delay (Max Drive), 40%–60% | tpv | 25 pF 50 pF | 1.55/1.42 1.93/1.81 | 2.25/2.08 2.77/2.58 | 3.50/3.31 4.24/3.99 | ns | 1 |
| Output Enable to Output Valid Delay (High Drive), 40%–60% | tpv | 25 pF 50 pF | 1.67/1.54 2.16/2.03 | 2.41/2.23 3.08/2.86 | 3.74/3.51 4.66/4.34 | ns | |
| Output Enable to Output Valid Delay (Standard Drive), 40%–60% | tpv | 25 pF 50 pF | 2.02/1.90 2.76/2.63 | 2.91/2.71 3.91/3.62 | 4.48/4.21 5.85/5.39 | ns | |
| Output Pad Slew Rate (Max Drive) | tps | 25 pF 50 pF | 0.96/1.40 0.54/0.83 | 1.54/2.10 0.85/1.24 | 2.30/3.00 1.26/1.70 | V/ns | 2 |
| Output Pad Slew Rate (High Drive) | tps | 25 pF 50 pF | 0.76/1.10 0.41/0.64 | 1.19/1.71 0.63/0.95 | 1.78/2.39 0.95/1.30 | V/ns | |
| Output Pad Slew Rate (Standard Drive) | tps | 25 pF 50 pF | 0.52/0.78 0.28/0.44 | 0.80/1.19 0.43/0.64 | 1.20/1.60 0.63/0.87 | V/ns | |

Table 18. Fast I/O AC Parameters for OVDD = 3.0–3.6 V (continued)

| | | | | | | | |
|---|------|----------------|-------------|-------------|-------------|-------|---|
| Output Pad di/dt (Max Drive) | didt | 25 pF 50 pF | 46 49 | 108 113 | 250 262 | mA/ns | 3 |
| Output Pad di/dt (High Drive) | didt | 25 pF 50 pF | 35 37 | 82 86 | 197 207 | mA/ns | |
| Output Pad di/dt (Standard Drive) | didt | 25 pF 50 pF | 22 23 | 52 55 | 116 121 | mA/ns | |
| Input Pad Propagation Delay without Hysteresis, 50%–50% | tpi | 1.6pF | 0.729/0.458 | 0.97/0.0649 | 1.404/0.97 | ns | 4 |
| Input Pad Propagation Delay with Hysteresis, 50%–50% | tpi | 1.6pF | 1.203/0.938 | 1.172/1.187 | 1.713/1.535 | ns | |
| Input Pad Propagation Delay without Hysteresis, 40%–60% | tpi | 1.6pF | 0.879/0.977 | 1.434/1.12 | 1.854/1.427 | ns | |
| Input Pad Propagation Delay with Hysteresis, 40%–60% | tpi | 1.6pF | 1.353/1.457 | 1.637/1.659 | 2.163/1.991 | ns | |
| Input Pad Transition Times without Hysteresis | trfi | 1.6pF | 0.16/0.12 | 0.23/0.18 | 0.33/0.29 | ns | |
| Input Pad Transition Times with Hysteresis | trfi | 1.6pF | 0.16/0.13 | 0.22/0.18 | 0.33/0.29 | ns | 5 |
| Maximum Input Transition Times | trm | — | — | — | — | ns | |

Note:

1. Maximum condition for tpr, tpo, and tpv: wcs model, 1.1 V, IO 3.0 V and 105 °C. Min condition for tpr, tpo, and tpv: bcs model, 1.3 V, IO 3.6 V and –40 °C. Input transition time from core is 1ns (20%–80%).
2. Minimum condition for tps: wcs model, 1.1 V, IO 3.0 V and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.
3. Maximum condition for tdit: bcs model, 1.3 V, IO 3.6 V and –40 °C.
4. Maximum condition for tpi and trfi: wcs model, 1.1 V, IO 3.0 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, IO 3.6 V and –40 °C. Input transition time from pad is 5ns (20%–80%).
5. Hysteresis mode is recommended for input with transition time greater than 25 ns.

3.5.3 DDR I/O AC Parameters

The DDR pad type is configured by the IOMUXC_SW_PAD_CTL_GRP_DDRTYPE register (see Chapter 4, “External Signals and Pin Multiplexing,” in the *i.MX25 Multimedia Applications Processor Reference Manual*).

3.5.3.1 DDR_TYPE = 00 Standard Setting I/O AC Parameters and Requirements

Table 19 shows AC parameters for mobile DDR I/O. These settings are suitable for mDDR and DDR2 1.8V ($\pm 5\%$) applications.

Table 19. AC Parameters for Mobile DDR I/O

| Parameter | Symbol | Load Condition | Min. Rise/Fall | Typ. | Max. Rise/Fall | Units | Notes |
|---|--------|----------------|------------------------|------------------------|-------------------------|-------|-------|
| Duty cycle | Fduty | — | 40 | 50 | 60 | % | — |
| Clock frequency | f | — | — | — | 133 | MHz | 1 |
| Output pad transition times (max. drive) | tpr | 25 pF 50 pF | 0.52/0.51 0.98/0.96 | 0.79/0.72 1.49/1.34 | 1.25/1.09 2.31/1.98 | ns | 1 |
| Output pad transition times (high drive) | tpr | 25 pF 50 pF | 1.13/1.10 2.15/2.10 | 1.74/1.55 3.28/2.92 | 2.71/2.30 5.11/4.31 | ns | |
| Output pad transition times (standard drive) | tpr | 25 pF 50 pF | 2.26/2.19 4.30/4.18 | 3.46/3.07 6.59/5.79 | 5.39/4.56 10.13/8.55 | ns | |
| Output pad propagation delay (max. drive), 50%–50% | tpo | 15 pF 35 pF | 0.80/1.03 1.06/1.32 | 1.36/1.50 1.76/1.90 | 2.21/2.40 2.83/2.82 | ns | 1 |
| Output pad propagation delay (high drive), 50%–50% | tpo | 15 pF 35 pF | 1.04/1.27 1.63/1.90 | 1.74/1.83 2.63/2.69 | 2.79/2.70 4.18/3.86 | ns | |
| Output pad propagation delay (standard drive), 50%–50% | tpo | 15 pF 35 pF | 1.55/1.80 2.72/3.06 | 2.53/2.57 4.31/4.29 | 4.03/3.76 6.80/6.19 | ns | |
| Output pad propagation delay (max. drive), 40%–60% | tpo | 15 pF 35 pF | 0.80/0.91 1.06/1.12 | 1.44/1.59 1.76/1.91 | 2.24/2.29 2.74/2.75 | ns | 1 |
| Output pad propagation delay (high drive), 40%–60% | tpo | 15 pF 35 pF | 1.04/1.09 1.63/1.56 | 1.73/1.83 2.43/2.52 | 2.69/2.62 3.79/3.62 | ns | |
| Output pad propagation delay (standard drive), 40%–60% | tpo | 15 pF 35 pF | 1.50/1.74 2.73/2.42 | 2.36/2.41 3.77/3.78 | 3.67/3.46 5.86/5.37 | ns | |
| Output enable to output valid delay (max. drive), 50%–50% | tpv | 15 pF 35 pF | 1.17/1.01 1.43/1.30 | 1.93/1.61 2.33/2.00 | 3.06/2.55 3.69/3.13 | ns | 1 |
| Output enable to output valid delay (high drive), 50%–50% | tpv | 15 pF 35 pF | 1.38/1.28 1.97/1.92 | 2.25/1.99 3.16/2.86 | 3.58/3.10 5.01/4.39 | ns | |
| Output enable to output valid delay (standard drive), 50%–50% | tpv | 15 pF 35 pF | 1.92/1.57 3.12/3.16 | 3.11/2.79 4.97/4.59 | 4.98/4.13 7.97/6.98 | ns | |
| Output enable to output valid delay (max. drive), 40%–60% | tpv | 15 pF 35 pF | 1.28/1.12 1.49/1.36 | 2.01/1.70 2.33/2.01 | 3.09/2.60 3.60/3.06 | ns | 1 |
| Output enable to output valid delay (high drive), 40%–60% | tpv | 15 pF 35 pF | 1.43/1.33 1.90/1.84 | 2.24/1.99 2.96/2.68 | 3.47/3.02 4.59/4.03 | ns | |
| Output enable to output valid delay (standard drive), 40%–60% | tpv | 15 pF 35 pF | 1.85/1.78 2.80/2.81 | 2.91/2.62 4.37/4.53 | 4.54/3.96 6.88/6.05 | ns | |

Table 19. AC Parameters for Mobile DDR I/O (continued)

| Parameter | Symbol | Load Condition | Min. Rise/Fall | Typ. | Max. Rise/Fall | Units | Notes |
|---------------------------------------|--------|----------------|------------------------|------------------------|------------------------|-------|-------|
| Output pad slew rate (max. drive) | tps | 25 pF 50 pF | 0.80/0.92 0.43/0.50 | 1.35/1.50 0.72/0.81 | 2.23/2.27 1.66/1.68 | V/ns | 2 |
| Output pad slew rate (high drive) | tps | 25 pF 50 pF | 0.37/0.43 0.19/0.23 | 0.62/0.70 0.33/0.37 | 1.03/1.05 0.75/0.77 | V/ns | |
| Output pad slew rate (standard drive) | tps | 25 pF 50 pF | 0.18/0.22 0.10/0.12 | 0.31/0.35 0.16/0.18 | 0.51/0.53 0.38/0.39 | V/ns | |
| Output pad dl/dt (max. drive) | tdit | 25 pF 50 pF | 64 69 | 171 183 | 407 432 | mA/ns | 3 |
| Output pad dl/dt (high drive) | tdit | 25 pF 50 pF | 37 39 | 100 106 | 232 246 | mA/ns | |
| Output pad di/dt (standard drive) | tdit | 25 pF 50 pF | 18 20 | 50 52 | 116 123 | mA/ns | |
| Input pad transition times | trfi | 1.0 pF | 0.07/0.08 | 0.11/0.13 | 0.16/0.20 | ns | 4 |
| Input pad propagation delay, 50%–50% | tpi | 1.0 pF | 0.77/1.00 | 1.22/1.45 | 1.89/2.21 | ns | |
| Input pad propagation delay, 40%–60% | tpi | 1.0 pF | 1.59/1.82 | 2.04/2.27 | 2.69/3.01 | ns | |

Note:

1. Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from core is 1 ns (20%–80%).
2. Minimum condition for tps: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.
3. Maximum condition for tdit: bcs model, 1.3 V, I/O 1.95 V, and –40 °C.
4. Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 1.65 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

Table 20 shows the AC parameters for mobile DDR pbijtov18_33_ddr_clk I/O.

Table 20. AC Parameters for Mobile DDR pbijtov18_33_ddr_clk I/O

| Parameter | Symbol | Load Condition | Min. Rise/Fall | Typ. | Max. Rise/Fall | Units | Notes |
|--|--------|----------------|------------------------|------------------------|-------------------------|-------|-------|
| Duty cycle | Fduty | — | 40 | 50 | 60 | % | — |
| Clock frequency | f | — | — | — | 133 | MHz | 1 |
| Output pad transition times (max. drive) | tpr | 25 pF 50 pF | 0.52/0.51 0.98/0.96 | 0.79/0.72 1.49/1.34 | 1.25/1.09 2.31/1.98 | ns | 1 |
| Output pad transition times (high drive) | tpr | 25 pF 50 pF | 1.13/1.10 2.15/2.10 | 1.74/1.55 3.28/2.92 | 2.71/2.30 5.11/4.31 | ns | |
| Output pad transition times (standard drive) | tpr | 25 pF 50 pF | 2.26/2.19 4.30/4.18 | 3.46/3.07 6.59/5.79 | 5.39/4.56 10.13/8.55 | ns | |

Table 20. AC Parameters for Mobile DDR pbijtov18_33_ddr_clk I/O (continued)

| Parameter | Symbol | Load Condition | Min. Rise/Fall | Typ. | Max. Rise/Fall | Units | Notes |
|---|--------|----------------|------------------------|------------------------|------------------------|-------|-------|
| Output pad propagation delay (max. drive), 50%–50% input signals and crossing of output signals | tpo | 15 pF 35 pF | 1.28/1.19 1.56/1.47 | 1.97/1.83 2.37/2.23 | 2.98/2.78 3.57/3.37 | ns | 1 |
| Output pad propagation delay (high drive), 50%–50% input signals and crossing of output signals | tpo | 15 pF 35 pF | 1.54/1.43 2.14/2.04 | 2.34/2.20 3.22/3.08 | 3.54/3.33 4.85/4.65 | ns | |
| Output pad propagation delay (standard drive), 50%–50% input signals and crossing of output signals | tpo | 15 pF 35 pF | 2.05/1.94 3.27/3.16 | 3.11/2.96 4.86/4.72 | 4.70/4.50 7.33/7.12 | ns | |
| Output pad propagation delay (max. drive), 40%–60% input signals and crossing of output signals | tpo | 15 pF 35 pF | 1.45/1.36 1.73/1.64 | 2.13/2.00 2.53/2.40 | 3.14/2.94 3.74/3.54 | ns | 1 |
| Output pad propagation delay (high drive), 40%–60% input signals and crossing of output signals | tpo | 15 pF 35 pF | 1.70/1.60 2.31/2.21 | 2.51/2.37 3.38/3.24 | 3.70/3.50 5.02/4.82 | ns | |
| Output pad propagation delay (standard drive), 40%–60% input signals and crossing of output signals | tpo | 15 pF 35 pF | 2.22/2.11 3.43/3.32 | 3.27/3.13 5.02/4.88 | 4.87/4.66 7.49/7.29 | ns | |
| Output enable to output valid delay (max. drive), 50%–50% | tpv | 15 pF 35 pF | 1.16/1.12 1.42/1.41 | 1.91/1.81 2.31/2.20 | 3.10/2.89 3.72/3.47 | ns | 1 |
| Output enable to output valid delay (high drive), 50%–50% | tpv | 15 pF 35 pF | 1.39/1.39 1.98/2.02 | 2.28/2.18 3.18/3.04 | 3.69/3.43 5.08/4.69 | ns | |
| Output enable to output valid delay (standard drive), 50%–50% | tpv | 15 pF 35 pF | 1.90/1.94 3.07/3.20 | 3.09/2.94 4.88/4.66 | 4.95/4.55 7.73/7.05 | ns | |
| Output enable to output valid delay (max. drive), 40%–60% | tpv | 15 pF 35 pF | 1.28/1.24 1.49/1.47 | 2.00/1.90 2.32/2.21 | 3.14/2.93 3.64/3.41 | ns | 1 |
| Output enable to output valid delay (high drive), 40%–60% | tpv | 15 pF 35 pF | 1.45/1.44 1.92/1.95 | 2.28/2.19 2.99/2.87 | 3.60/3.36 4.69/4.36 | ns | |
| Output enable to output valid delay (standard drive), 40%–60% | tpv | 15 pF 35 pF | 1.85/1.88 2.78/2.88 | 2.92/2.79 4.34/4.16 | 4.58/4.25 6.79/6.24 | ns | |
| Output pad slew rate (max. drive) | tps | 25 pF 50 pF | 0.37/0.45 0.30/0.36 | 0.64/0.79 0.52/0.61 | 1.14/1.36 0.90/1.02 | V/ns | 2 |
| Output pad slew rate (high drive) | tps | 25 pF 50 pF | 0.30/0.37 0.21/0.25 | 0.51/0.63 0.36/0.42 | 0.91/1.06 0.63/0.67 | V/ns | |
| Output pad slew rate (standard drive) | tps | 25 pF 50 pF | 0.22/0.26 0.13/0.16 | 0.37/0.44 0.23/0.26 | 0.65/0.72 0.39/0.40 | V/ns | |

Table 20. AC Parameters for Mobile DDR pbijtov18_33_dds_clk I/O (continued)

| Parameter | Symbol | Load Condition | Min. Rise/Fall | Typ. | Max. Rise/Fall | Units | Notes |
|--------------------------------------|--------|----------------|----------------|------------|----------------|-------|-------|
| Output pad dl/dt (max. drive) | tdit | 25 pF 50 pF | 65 70 | 171 183 | 426 450 | mA/ns | 3 |
| Output pad dl/dt (high drive) | tdit | 25 pF 50 pF | 31 33 | 82 87 | 233 245 | mA/ns | |
| Output pad dl/dt (standard drive) | tdit | 25 pF 50 pF | 16 17 | 43 46 | 115 120 | mA/ns | |
| Input pad transition times | trfi | 1.0 pF | 0.07/0.08 | 0.11/0.13 | 0.16/0.20 | ns | 4 |
| Input pad propagation delay, 50%–50% | tpi | 1.0 pF | 0.84/0.84 | 1.40/1.34 | 2.25/2.16 | ns | |
| Input pad propagation delay, 40%–60% | tpi | 1.0 pF | 1.66/1.66 | 2.22/2.16 | 3.06/2.97 | ns | |

Note:

1. Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from core is 1 ns (20%–80%).
2. Minimum condition for tps: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.
3. Maximum condition for tdit: bcs model, 1.3 V, I/O 1.95 V, and –40 °C.
4. Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 1.65 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

Table 21 shows the AC requirements for mobile DDR I/O.

Table 21. AC Requirements for Mobile DDR I/O

| Parameter | Symbol | Min. | Max. | Units |
|---|---------|--------------------------|--------------------------|-------|
| AC input logic high | VIH(ac) | $0.8 \times \text{OVDD}$ | $\text{OVDD}+0.3$ | V |
| AC input logic low | VIL(ac) | –0.3 | $0.2 \times \text{OVDD}$ | V |
| AC differential input voltage | Vid(ac) | $0.6 \times \text{OVDD}$ | $\text{OVDD}+0.6$ | V |
| AC differential cross point voltage for input | Vix(ac) | $0.4 \times \text{OVDD}$ | $\text{OVDD}+0.6$ | V |

3.5.3.2 DDR_TYPE = 01 SDRAM I/O AC Parameters and Requirements

Table 22 shows AC parameters for SDRAM I/O.

Table 22. AC Parameters for SDRAM I/O

| Parameter | Symbol | Load Condition | Min. Rise/Fall | Typ. | Max. Rise/Fall | Units | Notes |
|-----------------|--------|----------------|----------------|------|----------------|-------|-------|
| Duty cycle | Fduty | — | 40 | 50 | 60 | % | — |
| Clock frequency | f | — | — | — | 125 | MHz | 1 |

Table 22. AC Parameters for SDRAM I/O (continued)

| Parameter | Symbol | Load Condition | Min. Rise/Fall | Typ. | Max. Rise/Fall | Units | Notes |
|---|-----------------|----------------|------------------------|------------------------|-------------------------|-------|-------|
| Output pad transition times (max. drive) | tp _r | 25 pF 50 pF | 0.82/0.87 1.56/1.67 | 1.14/1.13 2.13/2.09 | 1.62/1.50 3.015/2.77 | ns | 1 |
| Output pad transition times (high drive) | tp _r | 25 pF 50 pF | 1.23/1.31 2.31/2.47 | 1.71/1.68 3.22/3.12 | 2.39/2.22 4.53/4.16 | ns | |
| Output pad transition times (standard drive) | tp _r | 25 pF 50 pF | 2.44/2.60 4.65/4.99 | 3.38/3.27 6.38/6.23 | 4.73/4.38 9.05/8.23 | ns | |
| Output pad propagation delay (max. drive), 50%–50% | tp _o | 15 pF 35 pF | 0.97/1.19 2.85/3.21 | 1.69/0.75 2.02/2.30 | 2.17/2.46 2.93/3.27 | ns | 1 |
| Output pad propagation delay (high drive), 50%–50% | tp _o | 15 pF 35 pF | 1.15/1.39 3.57/3.91 | 1.72/1.93 2.54/2.85 | 2.51/2.77 3.66/3.97 | ns | |
| Output pad propagation delay (standard drive), 50%–50% | tp _o | 15 pF 35 pF | 2.01/1.57 5.73/6.05 | 2.45/2.69 4.10/4.51 | 3.54/3.77 5.84/6.13 | ns | |
| Output pad propagation delay (max. drive), 40%–60% | tp _o | 15 pF 35 pF | 1.06/1.26 1.38/1.38 | 1.53/1.73 1.96/2.23 | 2.18/2.47 2.78/3.12 | ns | 1 |
| Output pad propagation delay (high drive), 40%–60% | tp _o | 15 pF 35 pF | 1.15/1.20 1.75/1.67 | 1.72/1.93 2.37/2.66 | 2.45/2.71 3.35/3.67 | ns | |
| Output pad propagation delay (standard drive), 40%–60% | tp _o | 15 pF 35 pF | 1.91/2.01 2.88/2.56 | 2.30/2.52 3.59/3.97 | 3.26/3.50 5.06/5.36 | ns | |
| Output enable to output valid delay (max. drive), 50%–50% | tp _v | 15 pF 35 pF | 0.90/1.27 1.07/1.77 | 1.44/1.89 1.66/2.51 | 2.19/2.87 2.51/3.69 | ns | 1 |
| Output enable to output valid delay (high drive), 50%–50% | tp _v | 15 pF 35 pF | 1.01/1.48 1.37/2.33 | 1.58/2.16 2.06/3.09 | 2.38/3.23 3.06/4.46 | ns | |
| Output enable to output valid delay (standard drive), 50%–50% | tp _v | 15 pF 35 pF | 1.32/2.14 2.04/3.67 | 2.02/3.00 3.00/4.91 | 3.01/4.36 4.40/6.90 | ns | |
| Output enable to output valid delay (max. drive), 40%–60% | tp _v | 15 pF 35 pF | 1.03/1.34 1.16/1.74 | 1.54/1.94 1.74/2.44 | 2.26/2.88 2.55/3.54 | ns | — |
| Output enable to output valid delay (high drive), 40%–60% | tp _v | 15 pF 35 pF | 1.11/1.51 1.39/2.10 | 1.65/2.15 2.03/2.89 | 2.43/3.16 2.95/4.13 | ns | |
| Output enable to output valid delay (standard drive), 40%–60% | tp _v | 15 pF 35 pF | 1.35/2.03 1.91/3.23 | 1.99/2.83 2.76/4.30 | 2.89/4.03 3.98/6.01 | ns | |
| Output pad slew rate (max. drive) | tp _s | 25 pF 50 pF | 1.11/1.20 0.97/0.65 | 1.74/1.75 0.92/0.94 | 2.42/2.46 1.39/1.30 | V/ns | 2 |
| Output pad slew rate (high drive) | tp _s | 25 pF 50 pF | 0.76/0.80 0.40/0.43 | 1.16/1.19 0.61/0.63 | 1.76/1.66 0.93/0.87 | V/ns | |
| Output pad slew rate (standard drive) | tp _s | 25 pF 50 pF | 0.38/0.41 0.20/0.22 | 0.59/0.60 0.31/0.32 | 0.89/0.82 0.47/0.43 | V/ns | |

Table 22. AC Parameters for SDRAM I/O (continued)

| Parameter | Symbol | Load Condition | Min. Rise/Fall | Typ. | Max. Rise/Fall | Units | Notes |
|--------------------------------------|--------|----------------|----------------|------------|----------------|-------|-------|
| Output pad dl/dt (max. drive) | tdit | 25 pF 50 pF | 89 94 | 198 209 | 398 421 | mA/ns | 3 |
| Output pad dl/dt (high drive) | tdit | 25 pF 50 pF | 59 62 | 132 139 | 265 279 | mA/ns | |
| Output pad dl/dt (standard drive) | tdit | 25 pF 50 pF | 29 31 | 65 69 | 132 139 | mA/ns | |
| Input pad transition times | trfi | 1.0 pF | 0.07/0.08 | 0.11/0.12 | 0.16/0.20 | ns | 4 |
| Input pad propagation delay, 50%–50% | tpi | 1.0 pF | 0.35/1.17 | 0.63/1.53 | 1.16/2.04 | ns | |
| Input pad propagation delay, 40%–60% | tpi | — | 1.18/1.99 | 1.45/2.35 | 1.97/2.85 | — | |

Note:

1. Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 3.0 V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 3.6 V and –40 °C. Input transition time from core is 1 ns (20%–80%).
2. Minimum condition for tps: wcs model, 1.1 V, I/O 3.0 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.
3. Maximum condition for tdit: bcs model, 1.3 V, I/O 3.6 V, and –40 °C.
4. Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 3.0 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 3.6 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

Table 23 shows AC parameters for SDRAM pbijtov18_33_ddr_clk I/O.

Table 23. AC Parameters for SDRAM pbijtov18_33_ddr_clk I/O

| Parameter | Symbol | Load Condition | Min. Rise/Fall | Typ. | Max. Rise/Fall | Units | Notes |
|---|--------|----------------|------------------------|------------------------|-------------------------|-------|-------|
| Duty cycle | Fduty | — | 40 | 50 | 60 | % | — |
| Clock frequency | f | — | — | — | 125 | MHz | 1 |
| Output pad transition times (max. drive) | tpr | 25 pF 50 pF | 0.82/0.87 1.56/1.67 | 1.14/1.13 2.13/2.09 | 1.62/1.50 3.015/2.77 | ns | 1 |
| Output pad transition times (high drive) | tpr | 25 pF 50 pF | 1.23/1.31 2.31/2.47 | 1.71/1.68 3.22/3.12 | 2.39/2.22 4.53/4.16 | ns | |
| Output pad transition times (standard drive) | tpr | 25 pF 50 pF | 2.44/2.60 4.65/4.99 | 3.38/3.27 6.38/6.23 | 4.73/4.38 9.05/8.23 | ns | |
| Output pad propagation delay (max. drive), 50%–50% input signals and crossing of output signals | tpo | 15 pF 35 pF | 1.50/1.40 1.95/1.85 | 2.23/2.07 2.81/2.66 | 3.28/3.04 4.06/3.82 | ns | 1 |
| Output pad propagation delay (high drive), 50%–50% input signals and crossing of output signals | tpo | 15 pF 35 pF | 1.69/1.59 2.35/2.25 | 2.48/2.32 3.35/3.19 | 3.63/3.38 4.80/4.56 | ns | |
| Output pad propagation delay (standard drive), 50%–50% input signals and crossing of output signals | tpo | 15 pF 35 pF | 2.26/2.15 3.59/3.49 | 3.24/3.08 4.98/4.82 | 4.66/4.42 7.00/6.75 | ns | |

Table 23. AC Parameters for SDRAM pbijtov18_33_ddr_clk I/O (continued)

| Parameter | Symbol | Load Condition | Min. Rise/Fall | Typ. | Max. Rise/Fall | Units | Notes |
|---|--------|----------------|------------------------|------------------------|------------------------|-------|-------|
| Output pad propagation delay (max. drive), 40%–60% input signals and crossing of output signals | tpo | 15 pF 35 pF | 1.67/1.57 2.11/2.02 | 2.39/2.24 2.97/2.82 | 3.45/3.21 4.23/3.99 | ns | 1 |
| Output pad propagation delay (high drive), 40%–60% input signals and crossing of output signals | tpo | 15 pF 35 pF | 1.85/1.75 2.52/2.42 | 2.65/2.49 3.51/3.36 | 3.79/3.55 4.97/4.72 | ns | |
| Output pad propagation delay (standard drive), 40%–60% input signals and crossing of output signals | tpo | 15 pF 35 pF | 2.42/2.32 3.76/3.66 | 3.40/3.25 5.15/4.99 | 4.83/4.59 7.17/6.92 | ns | |
| Output enable to output valid delay (max. drive), 50%–50% | tpv | 15 pF 35 pF | 1.37/1.34 1.77/1.83 | 2.22/2.02 2.77/2.63 | 3.53/3.12 4.30/3.92 | ns | 1 |
| Output enable to output valid delay (high drive), 50%–50% | tpv | 15 pF 35 pF | 1.55/1.56 2.15/2.29 | 2.46/2.30 3.28/3.21 | 3.87/3.47 5.02/4.67 | ns | |
| Output enable to output valid delay (standard drive), 50%–50% | tpv | 15 pF 35 pF | 2.07/2.18 3.28/3.65 | 3.20/3.08 4.84/4.90 | 4.92/4.50 7.21/6.89 | ns | |
| Output enable to output valid delay (max. drive), 40%–60% | tpv | 15 pF 35 pF | 1.46/1.42 1.77/1.81 | 2.28/2.07 2.71/2.56 | 3.54/3.13 4.15/3.78 | ns | |
| Output enable to output valid delay (high drive), 40%–60% | tpv | 15 pF 35 pF | 1.60/1.59 2.07/2.18 | 2.47/2.30 3.12/3.02 | 3.82/3.41 4.72/4.37 | ns | |
| Output enable to output valid delay (standard drive), 40%–60% | tpv | 15 pF 35 pF | 2.01/2.09 2.96/3.26 | 3.05/2.91 4.34/4.37 | 4.64/4.23 6.45/6.13 | ns | |
| Output pad slew rate (max. drive) | tps | 25 pF 50 pF | 1.11/1.20 0.60/0.65 | 1.74/1.75 0.93/0.95 | 2.63/2.48 1.39/1.29 | V/ns | 2 |
| Output pad slew rate (high drive) | tps | 25 pF 50 pF | 0.75/0.81 0.40/0.43 | 1.16/1.18 0.62/0.64 | 1.76/1.65 0.94/0.87 | V/ns | |
| Output pad slew rate (standard drive) | tps | 25 pF 50 pF | 0.38/0.41 0.20/0.22 | 0.59/0.61 0.31/0.32 | 0.89/0.83 0.47/0.43 | V/ns | |
| Output pad dl/dt (max. drive) | tdit | 25 pF 50 pF | 89 95 | 202 213 | 435 456 | mA/ns | 3 |
| Output pad dl/dt (high drive) | tdit | 25 pF 50 pF | 60 63 | 135 142 | 288 302 | mA/ns | |
| Output pad dl/dt (standard drive) | tdit | 25 pF 50 pF | 29 31 | 67 70 | 144 150 | mA/ns | |
| Input pad transition times | trfi | 1.0 pF | 0.07/0.08 | 0.11/0.12 | 0.16/0.20 | ns | 4 |
| Input pad propagation delay, 50%–50% | tpi | 1.0 pF | 0.56/0.69 | 0.87/1.08 | 1.37/1.62 | ns | |
| Input pad propagation delay, 40%–60% | tpi | | 1.38/1.51 | 1.68/1.89 | 2.18/2.42 | | |

Note:

1. Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 3.0 V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 3.6 V and –40 °C. Input transition time from core is 1 ns (20%–80%).
2. Minimum condition for tps: wcs model, 1.1 V, I/O 3.0 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

3. Maximum condition for tdit: bcs model, 1.3 V, I/O 3.6 V, and –40 °C.
4. Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 3.0 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 3.6 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

3.5.3.3 DDR_TYPE = 10 Max Setting I/O AC Parameters and Requirements

Table 24 shows AC parameters for DDR2 I/O.

Table 24. AC Parameters for DDR2 I/O

| Parameter | Symbol | Load Condition | Min. Rise/Fall | Typ. | Max. Rise/Fall | Units | Notes |
|--|--------|----------------|------------------------|------------------------|------------------------|-------|-------|
| Duty cycle | Fduty | — | 40 | 50 | 60 | % | — |
| Clock frequency | f | — | — | — | 133 | MHz | — |
| Output pad transition times | tpr | 25 pF 50 pF | 0.53/0.52 1.01/0.98 | 0.80/0.72 1.49/1.34 | 1.19/1.04 2.21/1.90 | ns | 1 |
| Output pad propagation delay, 50%–50% | tpo | 25 pF 50 pF | 0.93/1.25 1.26/1.54 | 1.56/1.70 2.07/2.19 | 2.52/2.53 3.29/3.24 | ns | 1 |
| Output pad propagation delay, 40%–60% | tpo | 25 pF 50 pF | 1.01/1.17 1.27/1.53 | 1.60/1.75 2.00/2.14 | 2.49/2.52 3.11/3.10 | ns | 1 |
| Output enable to output valid delay, 50%–50% | tpv | 25 pF 50 pF | 1.30/1.19 1.62/1.54 | 2.17/1.81 2.56/2.29 | 3.35/2.84 3.35/2.54 | ns | 1 |
| Output enable to output valid delay, 40%–60% | tpv | 25 pF 50 pF | 1.39/1.27 1.64/1.55 | 2.13/1.86 2.62/2.23 | 3.38/2.83 4.14/2.38 | ns | 1 |
| Output pad slew rate | tps | 25 pF 50 pF | 0.86/0.98 0.46/0.54 | 1.35/1.5 0.72/0.81 | 2.15/2.19 1.12/1.16 | V/ns | 2 |
| Output pad dl/dt | tdit | 25 pF 50 pF | 65 70 | 157 167 | 373 396 | mA/ns | 3 |
| Input pad transition times | trfi | 1.0 pF | 0.07/0.08 | 0.10/0.12 | 0.17/0.20 | ns | 4 |
| Input pad propagation delay, 50%–50% | tpi | 1.0 pF | 0.83/0.99 | 1.23/1.49 | 1.79/2.04 | ns | |
| Input pad propagation delay, 40%–60% | tpi | 1.0 pF | 1.65/1.81 | 2.05/2.31 | 2.60/2.84 | ns | |

Note:

1. Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 1. V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 1.9 V and –40 °C. Input transition time from core is 1 ns (20%–80%).
2. Minimum condition for tps: wcs model, 1.1 V, I/O 1.7 V, and 105 °C. tps is measured between VIH to VIH for rising edge and between VIH to VIL for falling edge.
3. Maximum condition for tdit: bcs model, 1.3 V, I/O 1.9 V, and –40 °C.
4. Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 1.7 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 1.9 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

Table 25 shows AC parameters for DDR2 pbijtov18_33_dds_clk I/O.

Table 25. AC Parameters for DDR2 pbijtov18_33_dds_clk I/O

| Parameter | Symbol | Load Condition | Min. Rise/Fall | Typ. | Max. Rise/Fall | Units | Notes |
|--|--------|----------------|------------------------|------------------------|-------------------------|-------|-------|
| Duty cycle | Fduty | — | 40 | 50 | 60 | % | — |
| Clock frequency | f | — | — | — | 133 | MHz | — |
| Output pad transition times | tpr | 25 pF 50 pF | 0.53/0.52 1.01/0.98 | 0.80/0.72 1.49/1.34 | 1.19/1.04 2.21/1.90 | ns | 1 |
| Output pad propagation delay, 50%–50% input signals and crossing of output signals | tpo | 25 pF 50 pF | 1.3/1.21 1.59/1.5 | 1.97/1.84 2.37/2.24 | 2.91/2.71 3.48/3.28 | ns | 1 |
| Output pad propagation delay, 40%–60% input signals and crossing of output signals | tpo | 25 pF 50 pF | 1.47/1.38 1.75/1.67 | 2.13/2.00 2.54/2.40 | 3.072/2.87 3.65/3.45 | ns | 1 |
| Output enable to output valid delay, 50%–50% | tpv | 25 pF 50 pF | 1.32/1.28 1.66/1.65 | 2.11/2.00 2.61/2.50 | 3.31/3.12 4.06/3.81 | ns | 1 |
| Output enable to output valid delay, 40%–60% | tpv | 25 pF 50 pF | 1.40/1.37 1.67/1.66 | 2.16/2.06 2.56/2.45 | 3.30/3.13 3.89/3.67 | ns | 1 |
| Output pad slew rate | tps | 25 pF 50 pF | 0.86/0.98 0.46/0.54 | 1.35/1.5 0.72/0.81 | 2.15/2.19 1.12/1.16 | V/ns | 2 |
| Output pad dl/dt | tdit | 25 pF 50 pF | 72 77 | 172 183 | 400 422 | mA/ns | 3 |
| Input pad transition times | trfi | 1.0 pF | 0.07/0.08 | 0.10/0.12 | 0.17/0.20 | ns | 4 |
| Input pad propagation delay, 50%–50% | tpi | 1.0 pF | 0.89/0.87 | 1.41/1.37 | 2.16/2.07 | ns | |
| Input pad propagation delay, 40%–60% | tpi | 1.0 pF | 1.71/1.69 | 2.22/2.18 | 2.98/2.88 | ns | |

Note:

1. Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 1. V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 1.9 V and –40 °C. Input transition time from core is 1 ns (20%–80%).
2. Minimum condition for tps: wcs model, 1.1 V, I/O 1.7 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.
3. Maximum condition for tdit: bcs model, 1.3 V, I/O 1.9 V, and –40 °C.
4. Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 1.7 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 1.9 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

Table 26 shows the AC requirements for DDR2 I/O.

Table 26. AC Requirements for DDR2 I/O

| Parameter ¹ | Symbol | Min. | Max. | Units |
|---|---------|---------------|----------------|-------|
| AC input logic high | VIH(ac) | OVDD/2 + 0.25 | OVDD + 0.3 | V |
| AC input logic low | VIL(ac) | –0.3 | OVDD/2 – 0.25 | V |
| AC differential input voltage ² | Vid(ac) | 0.5 | OVDD + 0.6 | V |
| AC differential cross point voltage for input ³ | Vix(ac) | OVDD/2–0.175 | OVDD/2 + 0.175 | V |
| AC differential cross point voltage for output ⁴ | Vox(ac) | OVDD/2–0.125 | OVDD/2 + 0.125 | V |

¹ Note that the Jedec SSTL_18 specification (JESD8-15a) for an SSTL interface for class II operation supersedes any specification in this document.

- 2 Vid(ac) specifies the input differential voltage $|V_{tr}-V_{cp}|$ required for switching, where V_{tr} is the “true” input signal and V_{cp} is the “complementary” input signal. The minimum value is equal to $V_{ih(ac)}-V_{il(ac)}$
- 3 The typical value of $V_{ix(ac)}$ is expected to be about $0.5 \times OVDD$, and $V_{ix(ac)}$ is expected to track variation of $OVDD$. $V_{ix(ac)}$ indicates the voltage at which differential input signal must cross.
- 4 The typical value of $V_{ox(ac)}$ is expected to be about $0.5 \times OVDD$ and $V_{ox(ac)}$ is expected to track variation in $OVDD$. $V_{ox(ac)}$ indicates the voltage at which differential output signal must cross. $C_{load} = 25 \text{ pF}$.

3.6 Module Timing and Electrical Parameters

This section contains the timing and electrical parameters for i.MX25 modules.

3.6.1 1-Wire Timing Parameters

Figure 7 shows the reset and presence pulses (RPP) timing for 1-Wire, and Table 27 lists the RPP timing parameters.

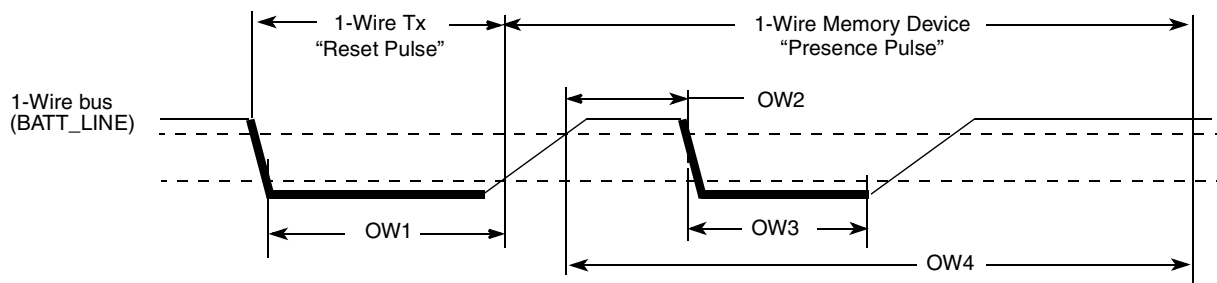


Figure 7. 1-Wire RPP Timing Diagram

Table 27. RPP Sequence Delay Comparisons Timing Parameters

| ID | Parameters | Symbol | Min. | Typ. | Max. | Units |
|-----|----------------------|------------|------|------|------|-------|
| OW1 | Reset Time Low | t_{RSTL} | 480 | 511 | — | us |
| OW2 | Presence Detect High | t_{PDH} | 15 | — | 60 | us |
| OW3 | Presence Detect Low | t_{PDL} | 60 | — | 240 | us |
| OW4 | Reset Time High | t_{RSTH} | 480 | 512 | — | us |

Figure 8 shows write 0 sequence timing, and Table 28 describes the timing parameters (OW5–OW6) that are shown in the figure.

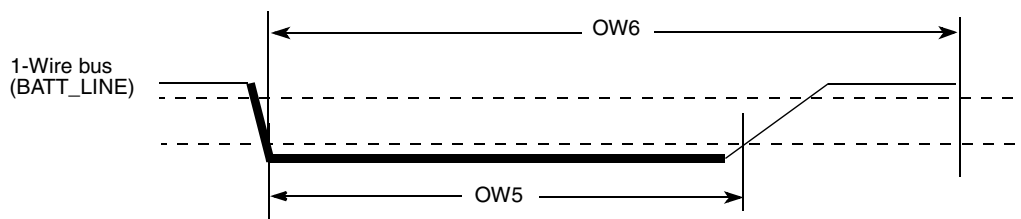


Figure 8. Write 0 Sequence Timing Diagram

Table 28. WR0 Sequence Timing Parameters

| ID | Parameter | Symbol | Min. | Typ. | Max. | Units |
|-----|------------------------|----------------|------|------|------|---------|
| OW5 | Write 0 Low Time | t_{WR0_low} | 60 | 100 | 120 | μs |
| OW6 | Transmission Time Slot | t_{SLOT} | OW5 | 117 | 120 | μs |

Figure 9 and Figure 10 show write 1 and read sequence timing, respectively. Table 29 describes the timing parameters (OW7–OW8) that are shown in the figure.

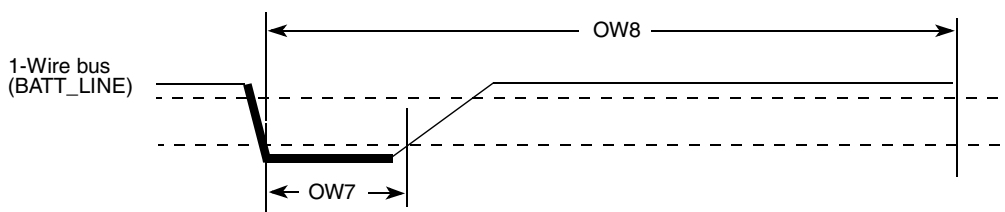


Figure 9. Write 1 Sequence Timing Diagram

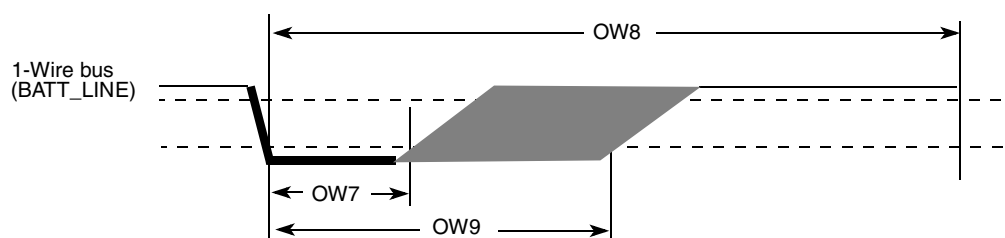


Figure 10. Read Sequence Timing Diagram

Table 29. WR1 /RD Timing Parameters

| ID | Parameter | Symbol | Min. | Typ. | Max. | Units |
|-----|-------------------------|---------------|------|------|------|---------|
| OW7 | Write 1 / read low time | t_{LOW1} | 1 | 5 | 15 | μs |
| OW8 | Transmission time slot | t_{SLOT} | 60 | 117 | 120 | μs |
| OW9 | Release time | $t_{RELEASE}$ | 15 | — | 45 | μs |

3.6.2 ATA Timing Parameters

Table 30 shows parameters used to specify the ATA timing. These parameters depend on the implementation of the ATA interface on silicon, the bus buffer used, the cable delay and cable skew.

Table 30. Timing Parameters

| Name | Description | Value/Contributing Factor | | | | | | | | | | |
|-------------------------------|---|--|-------------------------------|--------|-------|--------|-------------|------|-------|------|-------|------|
| T | Bus clock period | Peripheral clock frequency | | | | | | | | | | |
| ti_ds | Set-up time ata_data to ata_iordy edge (UDMA-in only) | <table style="margin-left: auto; margin-right: auto;"> <tr><td>UDMA0</td><td>15 ns</td></tr> <tr><td>UDMA1</td><td>10 ns</td></tr> <tr><td>UDMA2,UDMA3</td><td>7 ns</td></tr> <tr><td>UDMA4</td><td>5 ns</td></tr> <tr><td>UDMA5</td><td>4 ns</td></tr> </table> | UDMA0 | 15 ns | UDMA1 | 10 ns | UDMA2,UDMA3 | 7 ns | UDMA4 | 5 ns | UDMA5 | 4 ns |
| UDMA0 | 15 ns | | | | | | | | | | | |
| UDMA1 | 10 ns | | | | | | | | | | | |
| UDMA2,UDMA3 | 7 ns | | | | | | | | | | | |
| UDMA4 | 5 ns | | | | | | | | | | | |
| UDMA5 | 4 ns | | | | | | | | | | | |
| ti_dh | Hold time ata_iordy edge to ata_data (UDMA-in only) | <table style="margin-left: auto; margin-right: auto;"> <tr><td>UDMA0,UDMA1,UDMA2,UDMA3,UDMA4</td><td>5.0 ns</td></tr> <tr><td>UDMA5</td><td>4.6 ns</td></tr> </table> | UDMA0,UDMA1,UDMA2,UDMA3,UDMA4 | 5.0 ns | UDMA5 | 4.6 ns | | | | | | |
| UDMA0,UDMA1,UDMA2,UDMA3,UDMA4 | 5.0 ns | | | | | | | | | | | |
| UDMA5 | 4.6 ns | | | | | | | | | | | |
| tco | Propagation delay bus clock L-to-H to ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data, ata_buffer_en | 12.0 ns | | | | | | | | | | |
| tsu | Set-up time ata_data to bus clock L-to-H | 8.5 ns | | | | | | | | | | |
| tsui | Set-up time ata_iordy to bus clock H-to-L | 8.5 ns | | | | | | | | | | |
| thi | Hold time ata_iordy to bus clock H-to-L | 2.5 ns | | | | | | | | | | |
| tskew1 | Maximum difference in propagation delay bus clock L-to-H to any of the following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en | 7 ns | | | | | | | | | | |
| tskew2 | Maximum difference in buffer propagation delay for any of the following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en | Transceiver | | | | | | | | | | |
| tskew3 | Maximum difference in buffer propagation delay for any of the following signals ata_iordy, ata_data (read) | Transceiver | | | | | | | | | | |
| tbuf | Maximum buffer propagation delay | Transceiver | | | | | | | | | | |
| tcable1 | cable propagation delay for ata_data | Cable | | | | | | | | | | |
| tcable2 | cable propagation delay for control signals ata_dior, ata_diow, ata_iordy, ata_dmack | Cable | | | | | | | | | | |
| tskew4 | Maximum difference in cable propagation delay between ata_iordy and ata_data (read) | Cable | | | | | | | | | | |
| tskew5 | Maximum difference in cable propagation delay between (ata_dior, ata_diow, ata_dmack) and ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_data (write) | Cable | | | | | | | | | | |
| tskew6 | Maximum difference in cable propagation delay without accounting for ground bounce | Cable | | | | | | | | | | |

3.6.2.1 PIO Mode Timing Parameters

Figure 11 shows a timing diagram for PIO read mode.

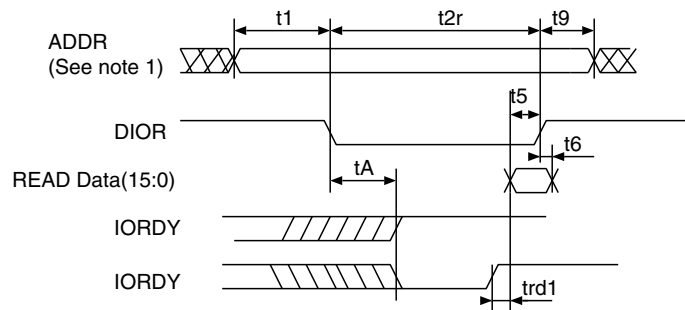


Figure 11. PIO Read Mode Timing

To meet PIO read mode timing requirements, a number of timing parameters must be controlled. Table 31 shows timing parameters and their determining relations, and indicates parameters that can be adjusted to meet required conditions.

Table 31. Timing Parameters for PIO Read Mode

| ATA Parameter | PIO Read Mode Timing Parameter ¹ | Relation | Adjustable Parameter |
|---------------|---|--|-----------------------------|
| t1 | t1 | $t1(\text{min.}) = \text{time_1} \times T - (\text{tskew1} + \text{tskew2} + \text{tskew5})$ | time_1 |
| t2 | t2r | $t2(\text{min.}) = \text{time_2r} \times T - (\text{tskew1} + \text{tskew2} + \text{tskew5})$ | time_2r |
| t9 | t9 | $t9(\text{min.}) = \text{time_9} \times T - (\text{tskew1} + \text{tskew2} + \text{tskew6})$ | time_9 |
| t5 | t5 | $t5(\text{min.}) = t_{co} + t_{su} + t_{buf} + t_{buf} + t_{cable1} + t_{cable2}$ | If not met, increase time_2 |
| t6 | t6 | 0 | — |
| tA | tA | $tA(\text{min.}) = (1.5 + \text{time_ax}) \times T - (t_{co} + t_{sui} + t_{cable2} + t_{cable2} + 2 \times t_{buf})$ | time_ax |
| trd | trd1 | $trd1(\text{max.}) = (-trd) + (\text{tskew3} + \text{tskew4})$ $trd1(\text{min.}) = (\text{time_pio_rdx} - 0.5) \times T - (t_{su} + t_{hi})$ $(\text{time_pio_rdx} - 0.5) \times T > t_{su} + t_{hi} + \text{tskew3} + \text{tskew4}$ | time_pio_rdx |
| t0 | — | $t0(\text{min.}) = (\text{time_1} + \text{time_2} + \text{time_9}) \times T$ | time_1, time_2r, time_9 |

¹ See Figure 11.

Figure 12 gives timing waveforms for PIO write mode.

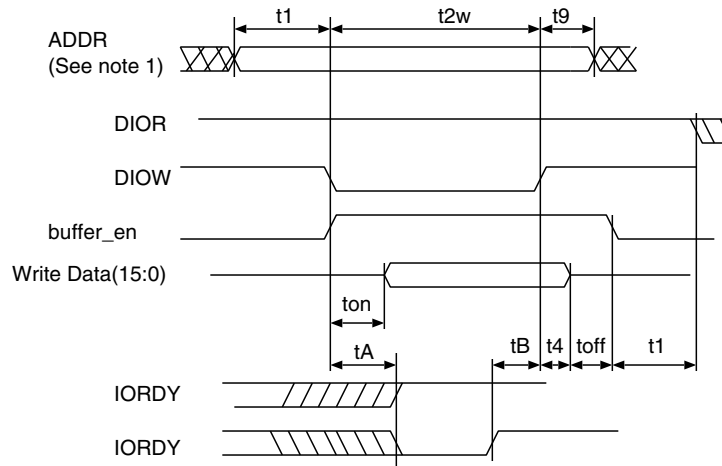


Figure 12. PIO Write Mode Timing

To meet PIO write mode timing requirements, a number of timing parameters must be controlled. Table 32 shows timing parameters and their determining relations, and indicates parameters that can be adjusted to meet required conditions.

Table 32. Timing Parameters for PIO Write Mode

| ATA Parameter | PIO Write Mode Timing Parameter ¹ | Relation | Adjustable Parameter(s) |
|---------------|--|---|------------------------------|
| t1 | t1 | $t1(\text{min.}) = \text{time_1} \times T - (\text{tskew1} + \text{tskew2} + \text{tskew5})$ | time_1 |
| t2 | t2w | $t2(\text{min.}) = \text{time_2w} \times T - (\text{tskew1} + \text{tskew2} + \text{tskew5})$ | time_2w |
| t9 | t9 | $t9(\text{min.}) = \text{time_9} \times T - (\text{tskew1} + \text{tskew2} + \text{tskew6})$ | time_9 |
| t3 | — | $t3(\text{min.}) = (\text{time_2w} - \text{time_on}) \times T - (\text{tskew1} + \text{tskew2} + \text{tskew5})$ | if not met, increase time_2w |
| t4 | t4 | $t4(\text{min.}) = \text{time_4} \times T - \text{tskew1}$ | time_4 |
| tA | tA | $tA = (1.5 + \text{time_ax}) \times T - (\text{tco} + \text{tsui} + \text{tcable2} + \text{tcable2} + 2 \times \text{tbuf})$ | time_ax |
| t0 | — | $t0(\text{min.}) = (\text{time_1} + \text{time_2} + \text{time_9}) \times T$ | time_1, time_2r, time_9 |
| — | — | Avoid bus contention when switching buffer on by making ton long enough | — |
| — | — | Avoid bus contention when switching buffer off by making toff long enough | — |

¹ See Figure 12.

3.6.2.2 Multiword DMA (MDMA) Mode Timing

Figure 13 and Figure 14 show the timing for MDMA read and write modes, respectively.

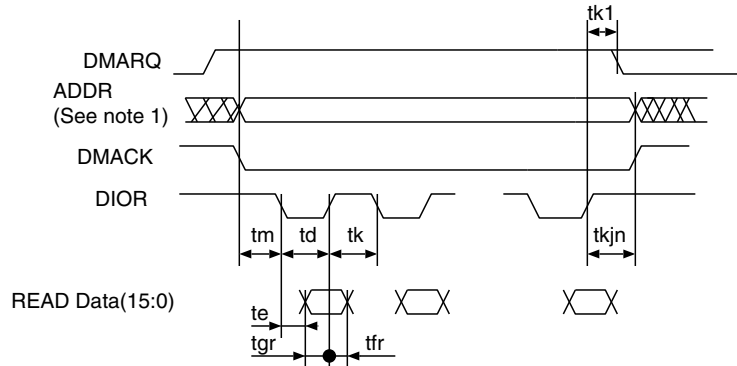


Figure 13. MDMA Read Mode Timing

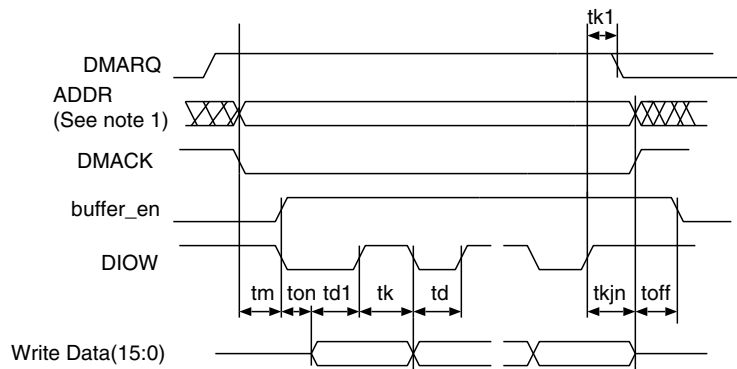


Figure 14. MDMA Write Mode Timing

To meet timing requirements, a number of timing parameters must be controlled. See Table 33 for details on timing parameters for MDMA read and write modes.

Table 33. Timing Parameters for MDMA Read and Write Modes

| ATA Parameter | MDMA Read ¹ and Write ² Timing Parameters | Relation | Adjustable Parameter(s) |
|---------------------|---|---|--------------------------------|
| t_m, t_i | t_m | $t_m(\text{min.}) = t_i(\text{min.}) = \text{time}_m \times T - (\text{tskew1} + \text{tskew2} + \text{tskew5})$ | time_m |
| t_d | t_d, t_{d1} | $t_{d1}(\text{min.}) = t_d(\text{min.}) = \text{time}_d \times T - (\text{tskew1} + \text{tskew2} + \text{tskew6})$ | time_d |
| t_k | t_k | $t_k(\text{min.}) = \text{time}_k \times T - (\text{tskew1} + \text{tskew2} + \text{tskew6})$ | time_k |
| t_0 | — | $t_0(\text{min.}) = (\text{time}_d + \text{time}_k) \times T$ | $\text{time}_d, \text{time}_k$ |
| $t_g(\text{read})$ | t_{gr} | $t_{gr}(\text{min.}-\text{read}) = t_{co} + t_{su} + t_{buf} + t_{buf} + t_{cable1} + t_{cable2}$ $t_{gr}(\text{min.}-\text{drive}) = t_d - t_e(\text{drive})$ | time_d |
| $t_f(\text{read})$ | t_{fr} | $t_{fr}(\text{min.}-\text{drive}) = 0 \text{ k}$ | — |
| $t_g(\text{write})$ | — | $t_g(\text{min.}-\text{write}) = \text{time}_d \times T - (\text{tskew1} + \text{tskew2} + \text{tskew5})$ | time_d |

Table 33. Timing Parameters for MDMA Read and Write Modes (continued)

| ATA Parameter | MDMA Read ¹ and Write ² Timing Parameters | Relation | Adjustable Parameter(s) |
|---------------|---|---|-----------------------------|
| tf(write) | — | $tf(\text{min.}-\text{write}) = \text{time_k} \times T - (\text{tskew1} + \text{tskew2} + \text{tskew6})$ | time_k |
| tL | — | $tL(\text{max.}) = (\text{time_d} + \text{time_k}-2) \times T - (\text{tsu} + \text{tco} + 2 \times \text{tbuf} + 2 \times \text{tcable2})$ | time_d, time_k ³ |
| tn, tj | tkjn | $tn = tj = tkjn = (\text{max.}(\text{time_k}, \text{time_jn}) \times T - (\text{tskew1} + \text{tskew2} + \text{tskew6}))$ | time_jn |
| — | ton toff | $ton = \text{time_on} \times T - \text{tskew1}$ $toff = \text{time_off} \times T - \text{tskew1}$ | — |

¹ See Figure 13.

² See Figure 14.

³ tk1 in the UDMA figures equals $(tk - 2 \times T)$.

3.6.2.3 Ultra DMA (UDMA) Mode Timing

UDMA mode timing is more complicated than PIO mode or MDMA mode. In this section, timing diagrams for UDMA in- and out-transfers are provided.

3.6.2.3.1 UDMA In-Transfer Timing

Figure 15 shows the timing for UDMA in-transfer start.

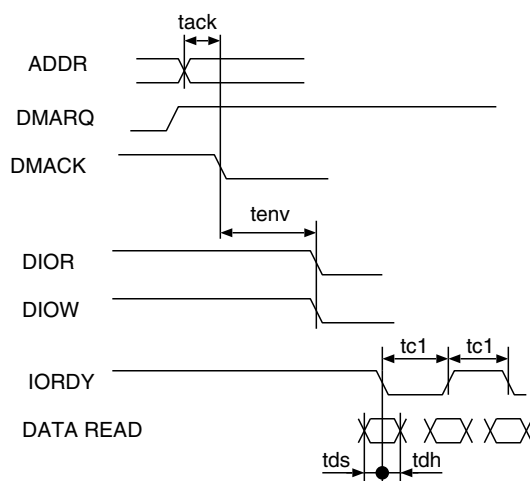


Figure 15. Timing for UDMA In-Transfer Start

Figure 16 shows the timing for host-terminated UDMA in-transfer.

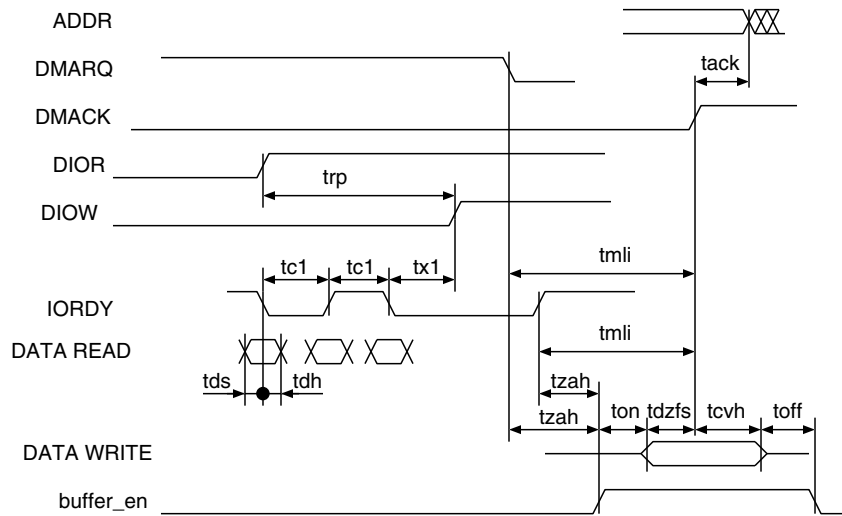


Figure 16. Timing for Host-Terminated UDMA In-Transfer

Figure 17 shows timing for device-terminated UDMA in-transfer.

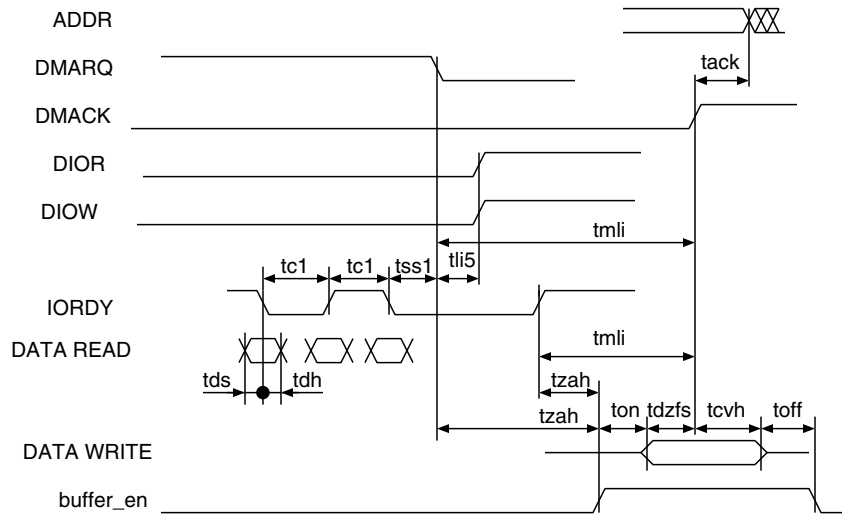


Figure 17. Timing for Device-Terminated UDMA Transfer

Timing parameters for UDMA in-burst are listed in Table 34.

Table 34. Timing Parameters for UDMA In-Burst

| ATA Parameter | Spec. Parameter | Value | Required Conditions |
|---------------|------------------|--|---|
| tack | tack | $tack(min.) = (time_ack \times T) - (tskew1 + tskew2)$ | time_ack |
| tenv | tenv | $tenv(min.) = (time_env \times T) - (tskew1 + tskew2)$ $tenv(max.) = (time_env \times T) + (tskew1 + tskew2)$ | time_env |
| tds | tds1 | $tds - (tskew3) - ti_ds > 0$ | tskew3, ti_ds, ti_dh should be low enough |
| tdh | tdh1 | $tdh - (tskew3) - ti_dh > 0$ | |
| tcyc | tc1 | $(tcyc - tskew) > T$ | T big enough |
| trp | trp | $trp(min.) = time_rp \times T - (tskew1 + tskew2 + tskew6)$ | time_rp |
| — | tx1 ¹ | $(time_rp \times T) - (tco + tsu + 3T + 2 \times tbuf + 2 \times tcable2) > trfs (drive)$ | time_rp |
| tmli | tmli1 | $tmli1(min.) = (time_mlix + 0.4) \times T$ | time_mlix |
| tzah | tzah | $tzah(min.) = (time_zah + 0.4) \times T$ | time_zah |
| tdzfs | tdzfs | $tdzfs = (time_dzfs \times T) - (tskew1 + tskew2)$ | time_dzfs |
| tcvh | tcvh | $tcvh = (time_cvh \times T) - (tskew1 + tskew2)$ | time_cvh |
| — | ton toff | $ton = time_on \times T - tskew1$ $toff = time_off \times T - tskew1$ | — |

¹ There is a special timing requirement in the ATA host that requires the internal DIOW to go only high three clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

Make t_{on} and t_{off} big enough to avoid bus contention.

3.6.2.4 UDMA Out-Transfer Timing

Figure 18 shows the timing for start of UDMA out-transfer.

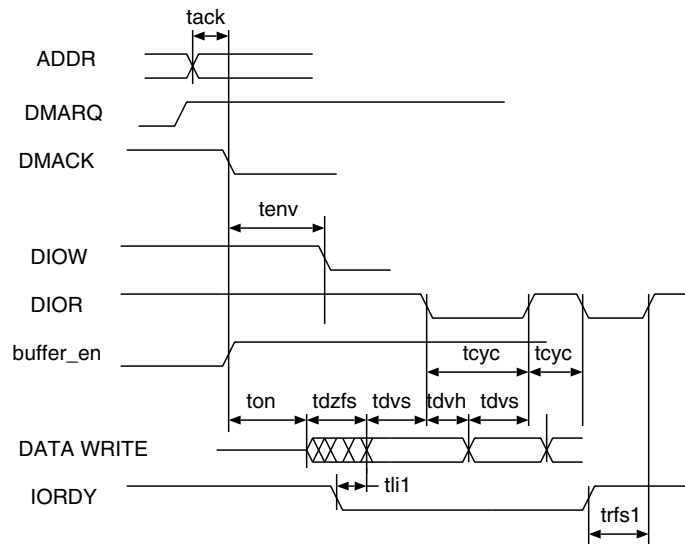


Figure 18. Timing for UDMA Out-Transfer Start

Figure 19 shows timing for host-terminated UDMA out-transfer.

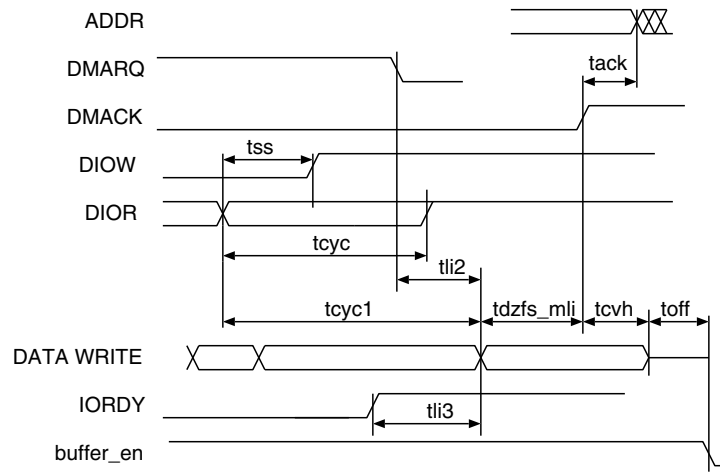


Figure 19. Timing for Host-Terminated UDMA Out-Transfer

Timing parameters for UDMA out-bursts are listed in Table 35.

Table 35. Timing Parameters UDMA Out-Bursts

| ATA Parameter | Spec Parameter | Value | How to Meet? |
|---------------|----------------|--|--------------|
| tack | tack | $tack(\text{min.}) = (\text{time_ack} \times T) - (\text{tskew1} + \text{tskew2})$ | time_ack |
| tenv | tenv | $tenv(\text{min.}) = (\text{time_env} \times T) - (\text{tskew1} + \text{tskew2})$ $tenv(\text{max.}) = (\text{time_env} \times T) + (\text{tskew1} + \text{tskew2})$ | time_env |
| tdvs | tdvs | $tdvs = (\text{time_dvs} \times T) - (\text{tskew1} + \text{tskew2})$ | time_dvs |
| tdvh | tdvh | $tdvs = (\text{time_dvh} \times T) - (\text{tskew1} + \text{tskew2})$ | time_dvh |
| tcyc | tcyc | $tcyc = \text{time_cyc} \times T - (\text{tskew1} + \text{tskew2})$ | time_cyc |
| t2cyc | — | $t2cyc = \text{time_cyc} \times 2 \times T$ | time_cyc |
| trfs1 | trfs | $trfs = 1.6 \times T + \text{tsui} + \text{tco} + \text{tbuf} + \text{tbuf}$ | — |
| — | tdzfs | $tdzfs = \text{time_dzfs} \times T - (\text{tskew1})$ | time_dzfs |
| tss | tss | $tss = \text{time_ss} \times T - (\text{tskew1} + \text{tskew2})$ | time_ss |
| tmli | tdzfs_mli | $tdzfs_mli = \max(\text{time_dzfs}, \text{time_mli}) \times T - (\text{tskew1} + \text{tskew2})$ | — |
| tli | tli1 | $tli1 > 0$ | — |
| tli | tli2 | $tli2 > 0$ | — |
| tli | tli3 | $tli3 > 0$ | — |
| tcvh | tcvh | $tcvh = (\text{time_cvh} \times T) - (\text{tskew1} + \text{tskew2})$ | time_cvh |
| — | ton toff | $ton = \text{time_on} \times T - \text{tskew1}$ $toff = \text{time_off} \times T - \text{tskew1}$ | — |

3.6.3 Digital Audio Mux (AUDMUX) Timing

The AUDMUX provides a programmable interconnect logic for voice, audio, and data routing between internal serial interfaces (SSI and SAP) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI modules. For more information, see [Section 3.6.17, “Synchronous Serial Interface \(SSI\) Timing.”](#)

3.6.4 CMOS Sensor Interface (CSI) Timing

The CSI enables the chip to connect directly to external CMOS image sensors, which are classified as dumb or smart as follows:

- Dumb sensors only support traditional sensor timing (vertical sync (VSYNC) and horizontal sync (HSYNC)) and output-only Bayer and statistics data.
- Smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats).

The following subsections describe the CSI timing in gated and ungated clock modes.

3.6.4.1 Gated Clock Mode Timing

[Figure 20](#) and [Figure 21](#) shows the gated clock mode timings for CSI, and [Table 36](#) describes the timing parameters (P1–P7) shown in the figures. A frame starts with a rising/falling edge on VSYNC, then HSYNC is asserted and holds for the entire line. The pixel clock is valid as long as HSYNC is asserted.

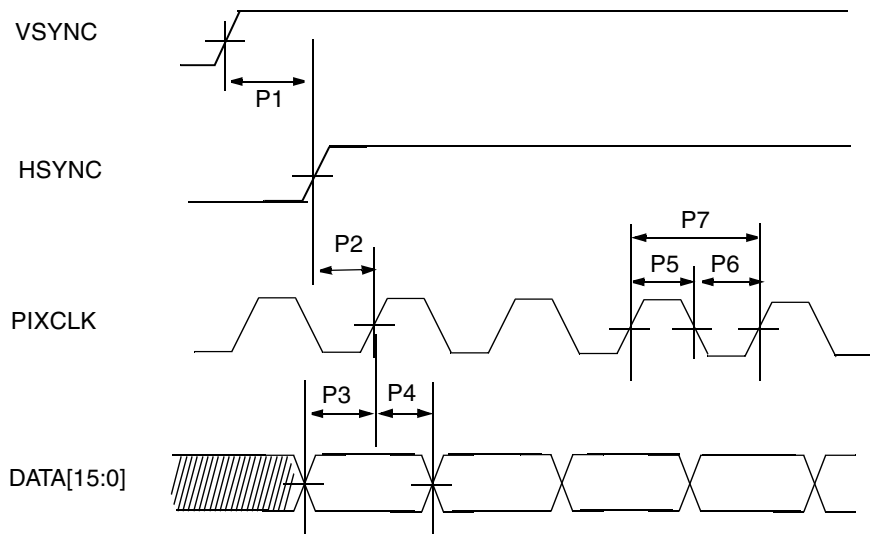


Figure 20. CSI Gated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

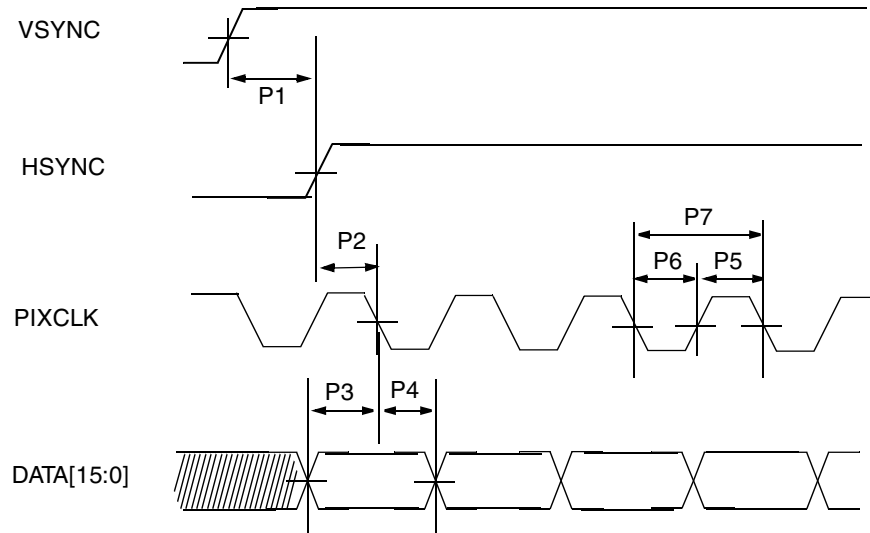


Figure 21. CSI Gated Clock Mode—Sensor Data at Rising Edge, Latch Data at Falling Edge

Table 36. CSI Gated Clock Mode Timing Parameters

| ID | Parameter | Symbol | Min. | Max. | Units |
|----|---------------------------|--------|------|----------------------------|-------|
| P1 | CSI VSYNC to HSYNC time | tV2H | 67.5 | — | ns |
| P2 | CSI HSYNC setup time | tHsu | 1 | — | ns |
| P3 | CSI DATA setup time | tDsu | 1 | — | ns |
| P4 | CSI DATA hold time | tDh | 1 | — | ns |
| P5 | CSI pixel clock high time | tCLKh | 10 | — | ns |
| P6 | CSI pixel clock low time | tCLKl | 10 | — | ns |
| P7 | CSI pixel clock frequency | fCLK | — | $48 \pm 10\%$ ¹ | MHz |

¹ Will be verified during qualification

3.6.4.2 Ungated Clock Mode Timing

Figure 22 shows the ungated clock mode timings of CSI, and Table 37 describes the timing parameters (P1–P6) that are shown in the figure. In ungated mode the VSYNC and PIXCLK signals are used, and the HSYNC signal is ignored.

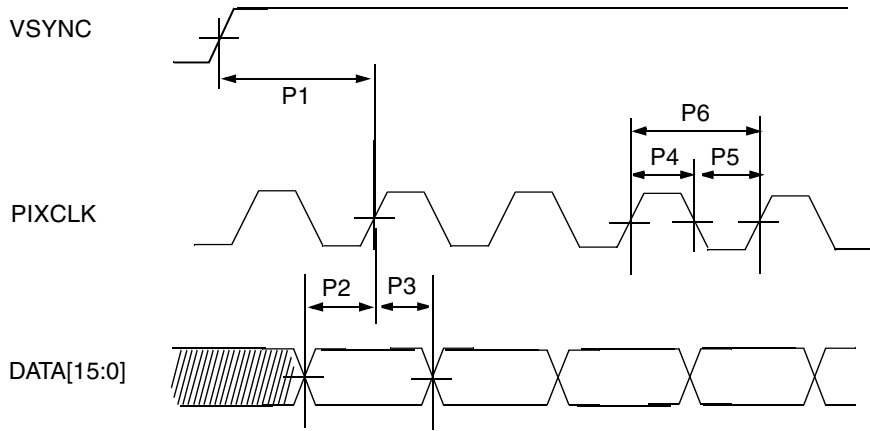


Figure 22. CSI Ungated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

Table 37. CSI Ungated Clock Mode Timing Parameters

| ID | Parameter | Symbol | Min. | Max. | Units |
|----|-------------------------------|--------|------|-----------------------|-------|
| P1 | CSI VSYNC to pixel clock time | tVSYNC | 67.5 | — | ns |
| P2 | CSI DATA setup time | tDsu | 1 | — | ns |
| P3 | CSI DATA hold time | tDh | 1 | — | ns |
| P4 | CSI pixel clock high time | tCLKh | 10 | — | ns |
| P5 | CSI pixel clock low time | tCLKl | 10 | — | ns |
| P6 | CSI pixel clock frequency | fCLK | — | 48 ± 10% ¹ | MHz |

¹ Will be verified during qualification

3.6.5 Configurable Serial Peripheral Interface (CSPI) Timing

Figure 23 and Figure 24 provide CSPI master and slave mode timing diagrams, respectively. Table 38 describes the timing parameters (t1–t14) that are shown in the figures. The values shown in timing diagrams were tested using a worst-case core voltage of 1.1 V, slow pad voltage of 2.68 V, and fast pad voltage of 1.65 V.

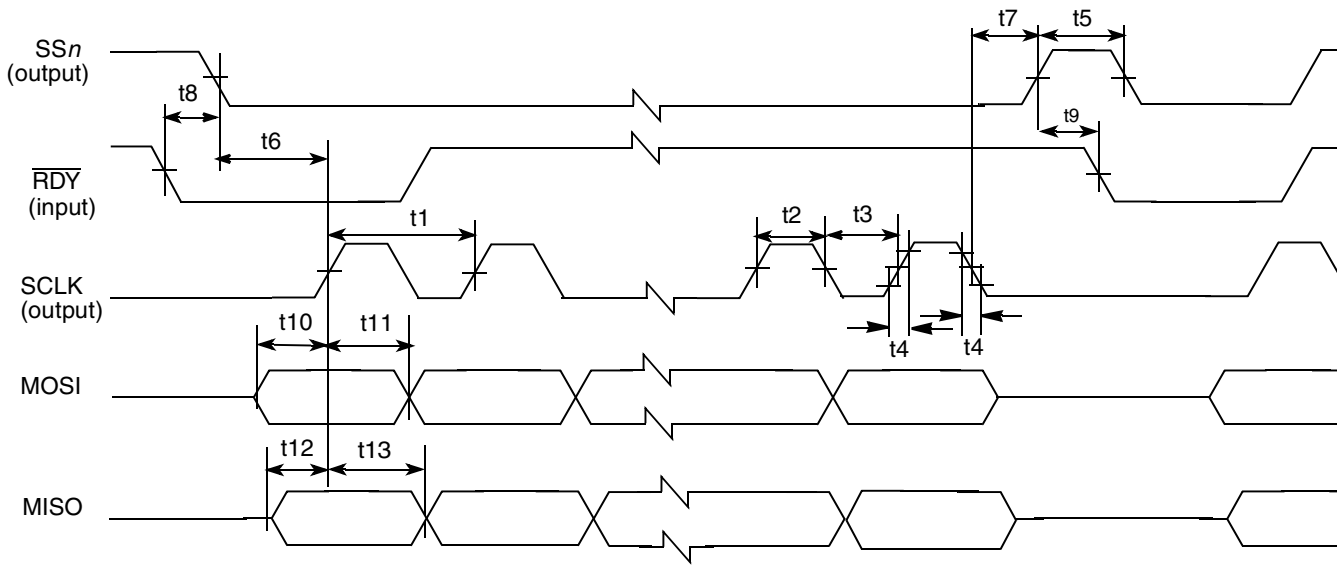


Figure 23. CSPI Master Mode Timing Diagram

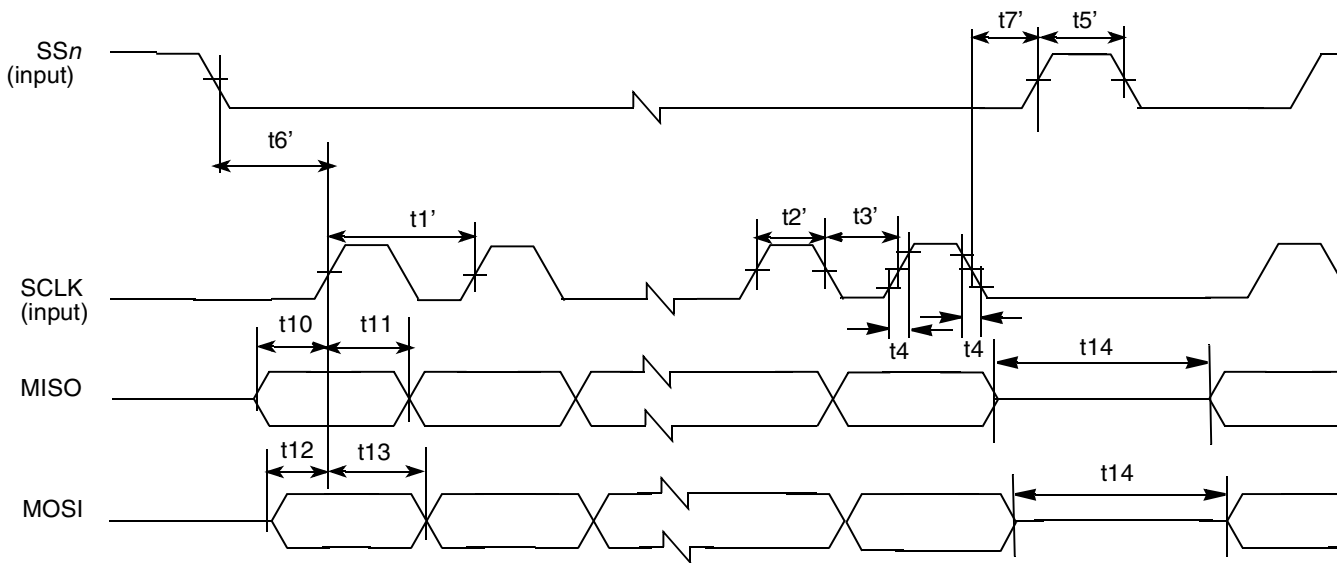


Figure 24. CSPI Slave Mode Timing Diagram

Table 38. CSPI Interface Timing Parameters

| ID | Parameter Description | Symbol | Minimum | Maximum | Units |
|-----|-----------------------------|-------------|---------|---------|-------|
| t1 | CSPI master SCLK cycle time | t_{clko} | 60.2 | — | ns |
| t2 | CSPI master SCLK high time | t_{clkoH} | 22.65 | — | ns |
| t3 | CSPI master SCLK low time | t_{clkoL} | 22.47 | — | ns |
| t1' | CSPI slave SCLK cycle time | t_{clki} | 60.2 | — | ns |
| t2' | CSPI slave SCLK high time | t_{clkiH} | 30.1 | — | ns |
| t3' | CSPI slave SCLK low time | t_{clkiL} | 30.1 | — | ns |

Table 38. CSPI Interface Timing Parameters (continued)

| ID | Parameter Description | Symbol | Minimum | Maximum | Units |
|-----|---|--------------|---|------------|-------|
| t4 | CSPI SCLK transition time | t_{pr}^1 | 2.6 | 8.5 | ns |
| t5 | SSn output pulse width | t_{WssO} | $2T_{sclk}^2 + T_{wait}^3$ | — | — |
| t5' | SSn input pulse width | t_{Wssi} | T_{per}^4 | — | — |
| t6 | SSn output asserted to first SCLK edge (SS output setup time) | t_{Ssso} | $3T_{sclk}$ | — | — |
| t6' | SSn input asserted to first SCLK edge (SS input setup time) | t_{Sssi} | T_{per} | — | — |
| t7 | CSPI master: Last SCLK edge to SSn negated (SS output hold time) | t_{Hsso} | $2T_{sclk}$ | — | — |
| t7' | CSPI slave: Last SCLK edge to SSn negated (SS input hold time) | t_{Hssi} | 30 | — | ns |
| t8 | CSPI master: CSPI1_RDY low to SSn asserted (CSPI1_RDY setup time) | t_{SrDY} | $2T_{per}$ | $5T_{per}$ | — |
| t9 | CSPI master: SSn negated to CSPI1_RDY low | t_{Hrdy} | 0 | — | ns |
| t10 | Output data setup time | t_{SdataO} | $(t_{clkoL} \text{ or } t_{clkoH} \text{ or } t_{clkiL} \text{ or } t_{clkiH}) - T_{ipg}^5$ | — | — |
| t11 | Output data hold time | t_{HdataO} | $t_{clkoL} \text{ or } t_{clkoH} \text{ or } t_{clkiL} \text{ or } t_{clkiH}$ | — | — |
| t12 | Input data setup time | t_{SdataI} | $T_{ipg} + 0.5$ | — | ns |
| t13 | Input data hold time | t_{HdataI} | 0 | — | ns |
| t14 | Pause between data word | t_{pause} | 0 | — | ns |

¹ The output SCLK transition time is tested with 25 pF drive.

² T_{sclk} = CSPI clock period

³ T_{wait} = Wait time, as specified in the sample period control register

⁴ T_{per} = CSPI reference baud rate clock period (PERCLK2)

⁵ T_{ipg} = CSPI main clock IPG_CLOCK period

3.6.6 External Memory Interface (EMI) Timing

The EMI module includes the enhanced SDRAM/LPDDR memory controller (ESDCTL), NAND Flash controller (NFC), and wireless external interface module (WEIM). The following subsections give timing information for these submodules.

3.6.6.1 ESDCTL Electrical Specifications

3.6.6.1.1 SDRAM Memory Controller

The following diagrams and tables specify the timings related to the SDRAMC module which interfaces SDRAM.

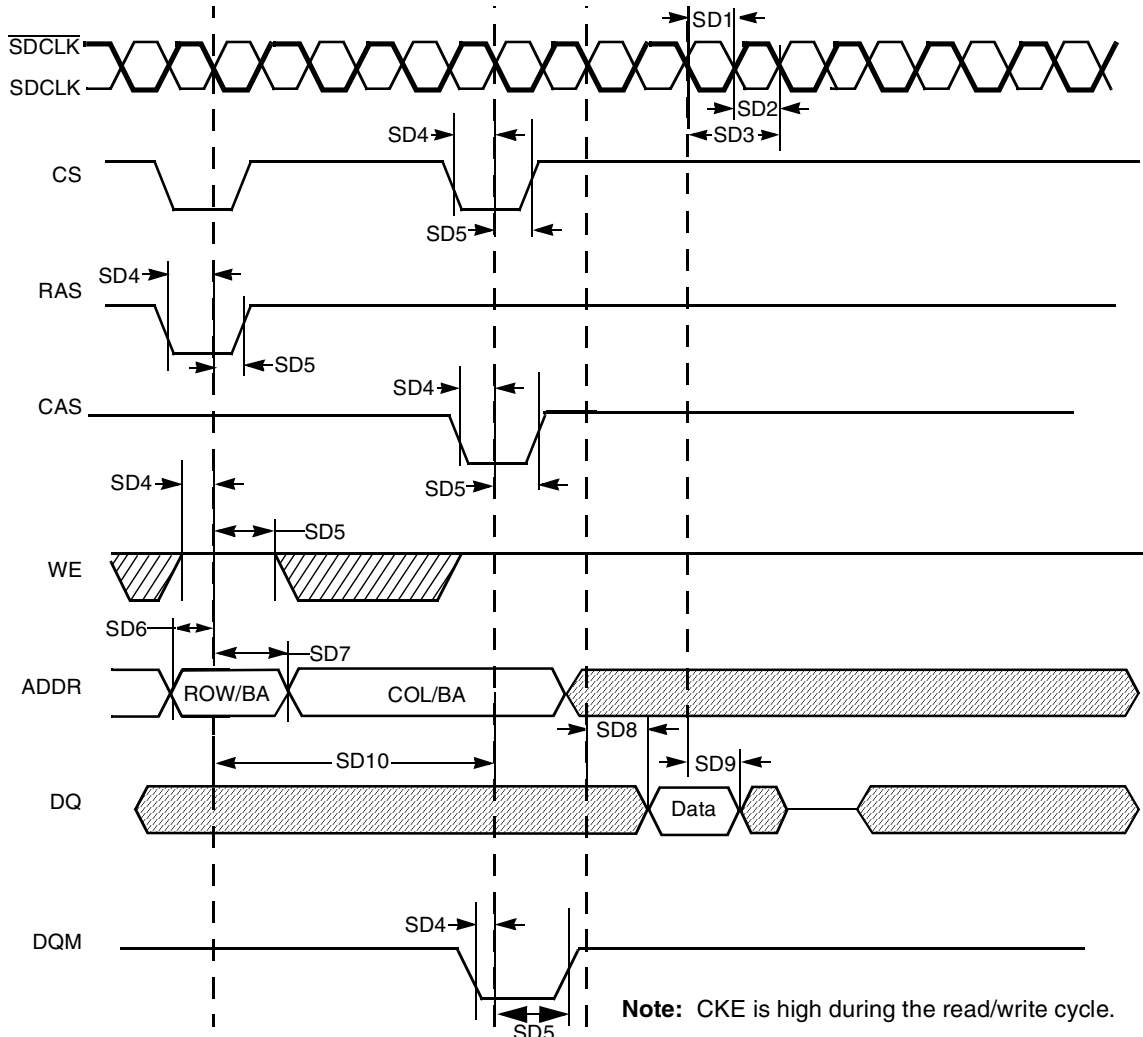


Figure 25. SDRAM Read Cycle Timing Diagram

Table 39. DDR/SDR SDRAM Read Cycle Timing Parameters

| ID | Parameter | Symbol | Min. | Max. | Unit |
|-----|---|------------------|------|------|------|
| SD1 | SDRAM clock high-level width ¹ | t _{CH} | 3.4 | 4.1 | ns |
| SD2 | SDRAM clock low-level width ¹ | t _{CL} | 3.4 | 4.1 | ns |
| SD3 | SDRAM clock cycle time | t _{CK} | 7.5 | — | ns |
| SD4 | CS, RAS, CAS, WE, DQM, CKE setup time | t _{CMS} | 2.0 | — | ns |
| SD5 | CS, RAS, CAS, WE, DQM, CKE hold time | t _{CMH} | 1.8 | — | ns |
| SD6 | Address setup time | t _{AS} | 2.0 | — | ns |
| SD7 | Address hold time | t _{AH} | 1.8 | — | ns |
| SD8 | SDRAM access time | t _{AC} | — | 6.47 | ns |

Table 39. DDR/SDR SDRAM Read Cycle Timing Parameters (continued)

| ID | Parameter | Symbol | Min. | Max. | Unit |
|------|-------------------------------------|--------|------|------|-------|
| SD9 | Data out hold time ² | tOH | 1.2 | — | ns |
| SD10 | Active to read/write command period | tRC | 10 | — | clock |

¹ SD1 + SD2 does not exceed 7.5 ns for 133 MHz.

² Timing parameters are relevant only to SDR SDRAM. For the specific DDR SDRAM data related timing parameters, see [Table 43](#) and [Table 44](#).

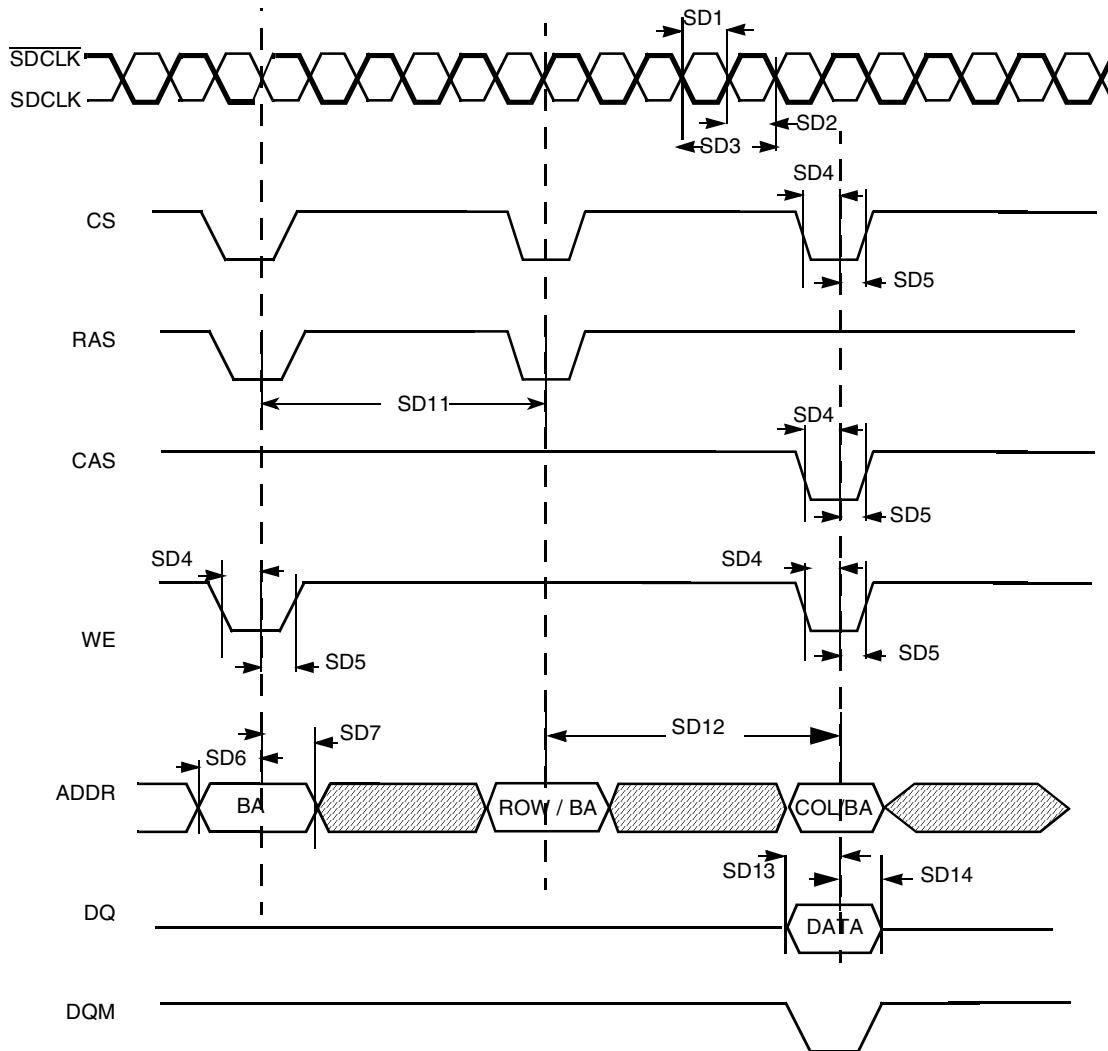


Figure 26. SDR SDRAM Write Cycle Timing Diagram

Table 40. SDR SDRAM Write Timing Parameters

| ID | Parameter | Symbol | Min. | Max. | Unit |
|------|---|--------|------|------|-------|
| SD1 | SDRAM clock high-level width | tCH | 3.4 | 4.1 | ns |
| SD2 | SDRAM clock low-level width | tCL | 3.4 | 4.1 | ns |
| SD3 | SDRAM clock cycle time | tCK | 7.5 | — | ns |
| SD4 | CS, RAS, CAS, WE, DQM, CKE setup time | tCMS | 2.0 | — | ns |
| SD5 | CS, RAS, CAS, WE, DQM, CKE hold time | tCMH | 1.8 | — | ns |
| SD6 | Address setup time | tAS | 2.0 | — | ns |
| SD7 | Address hold time | tAH | 1.8 | — | ns |
| SD11 | Precharge cycle period ¹ | tRP | 1 | 4 | clock |
| SD12 | Active to read/write command delay ¹ | tRCD | 1 | 8 | clock |
| SD13 | Data setup time | tDS | 2.0 | — | ns |
| SD14 | Data hold time | tDH | 1.3 | — | ns |

¹ SD11 and SD12 are determined by SDRAM controller register settings.

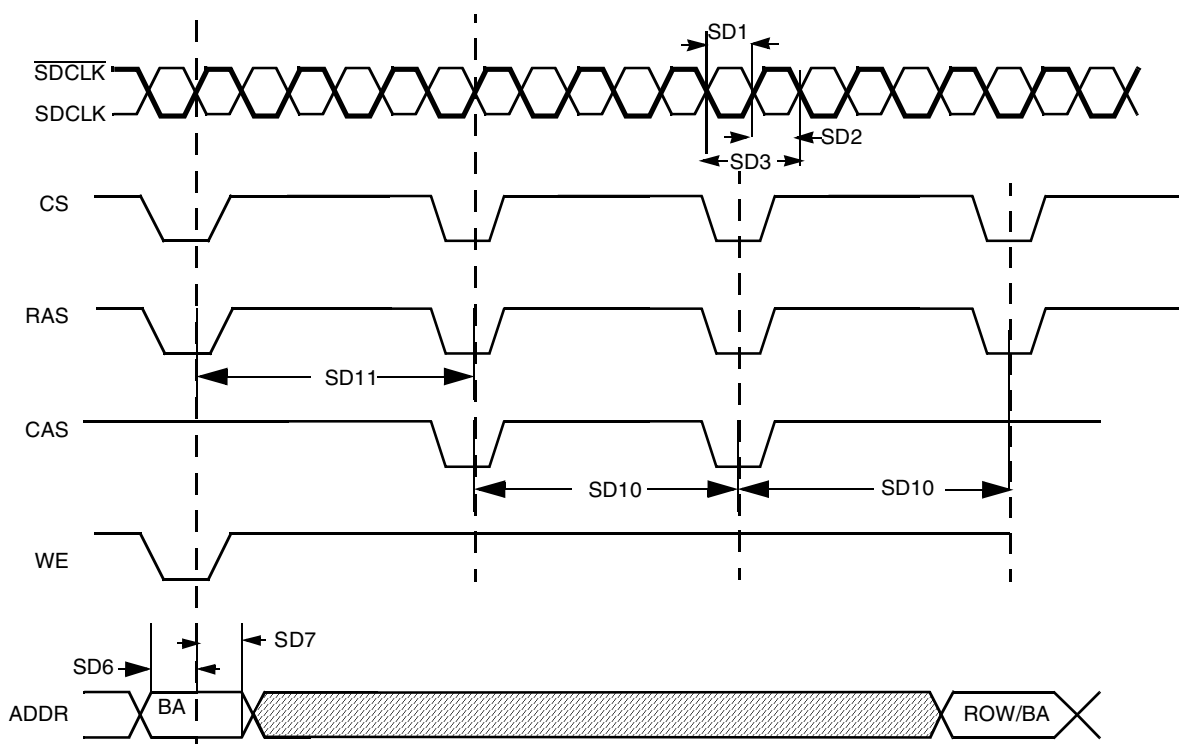


Figure 27. SDRAM Refresh Timing Diagram

Table 41. SDRAM Refresh Timing Parameters

| ID | Parameter | Symbol | Min. | Max. | Unit |
|------|--|--------|------|------|-------|
| SD1 | SDRAM clock high-level width | tCH | 3.4 | 4.1 | ns |
| SD2 | SDRAM clock low-level width | tCL | 3.4 | 4.1 | ns |
| SD3 | SDRAM clock cycle time | tCK | 7.5 | — | ns |
| SD6 | Address setup time | tAS | 1.8 | — | ns |
| SD7 | Address hold time | tAH | 1.8 | — | ns |
| SD10 | Precharge cycle period ¹ | tRP | 1 | 4 | clock |
| SD11 | Auto precharge command period ¹ | tRC | 2 | 20 | clock |

¹ SD10 and SD11 are determined by SDRAM controller register settings.

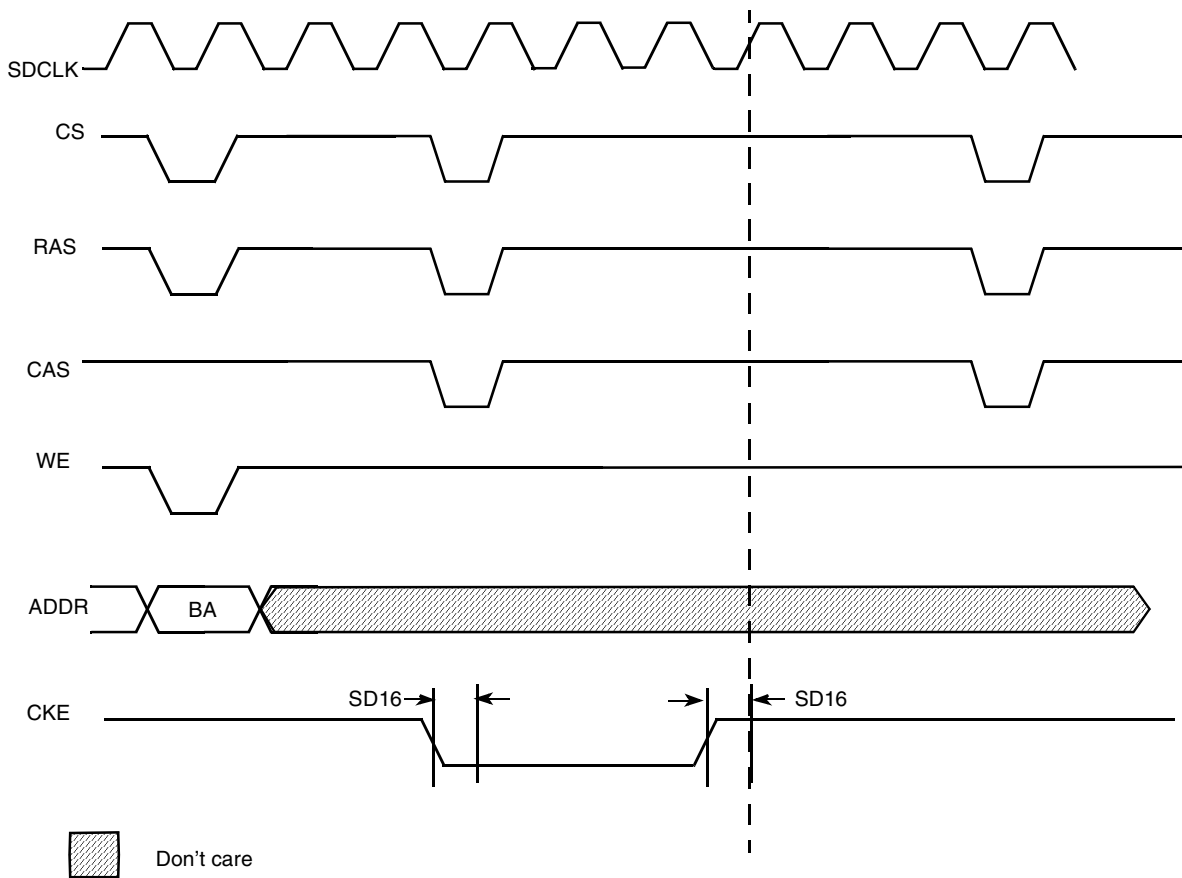


Figure 28. SDRAM Self-Refresh Cycle Timing Diagram

NOTE

The clock continues to run unless CKE is low. Then the clock is stopped in low state.

Table 42. SDRAM Self-Refresh Cycle Timing Parameters

| ID | Parameter | Symbol | Min. | Max. | Unit |
|------|-----------------------|--------|------|------|------|
| SD16 | CKE output delay time | tCKS | 1.8 | — | ns |

3.6.6.1.2 Mobile DDR SDRAM–Specific Parameters

The following diagrams and tables specify the timings related to the SDRAMC module which interfaces with the mobile DDR SDRAM.

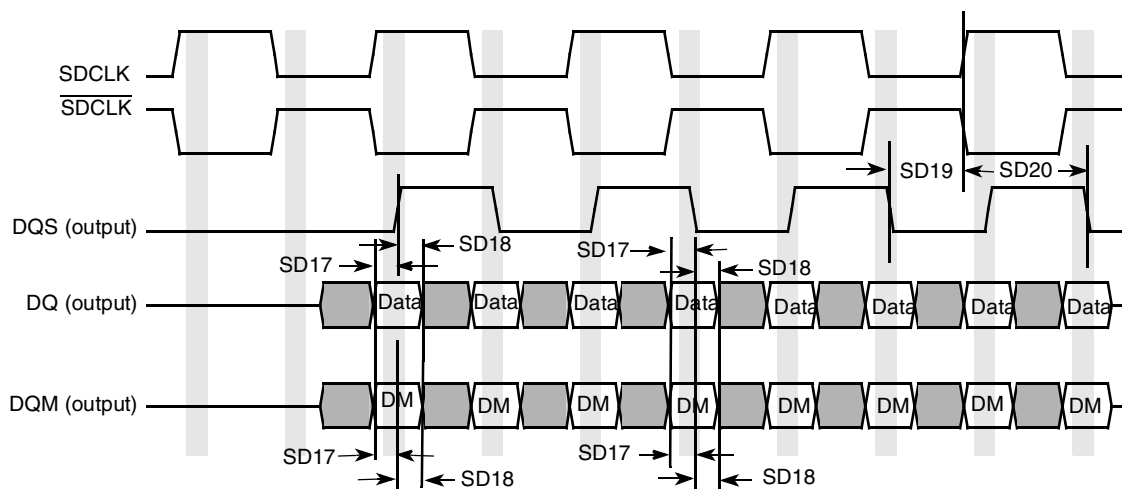


Figure 29. Mobile DDR SDRAM Write Cycle Timing Diagram

Table 43. Mobile DDR SDRAM Write Cycle Timing Parameters¹

| ID | Parameter | Symbol | Min. | Max. | Unit |
|------|---|--------|------|------|------|
| SD17 | DQ and DQM setup time to DQS | tDS | 0.95 | — | ns |
| SD18 | DQ and DQM hold time to DQS | tDH | 0.95 | — | ns |
| SD19 | Write cycle DQS falling edge to SDCLK output delay time | tDSS | 1.8 | — | ns |
| SD20 | Write cycle DQS falling edge to SDCLK output hold time | tDSH | 1.8 | — | ns |

¹ Test condition: Measured using delay line 5 programmed as follows: ESDCDLY5[15:0] = 0x0703.

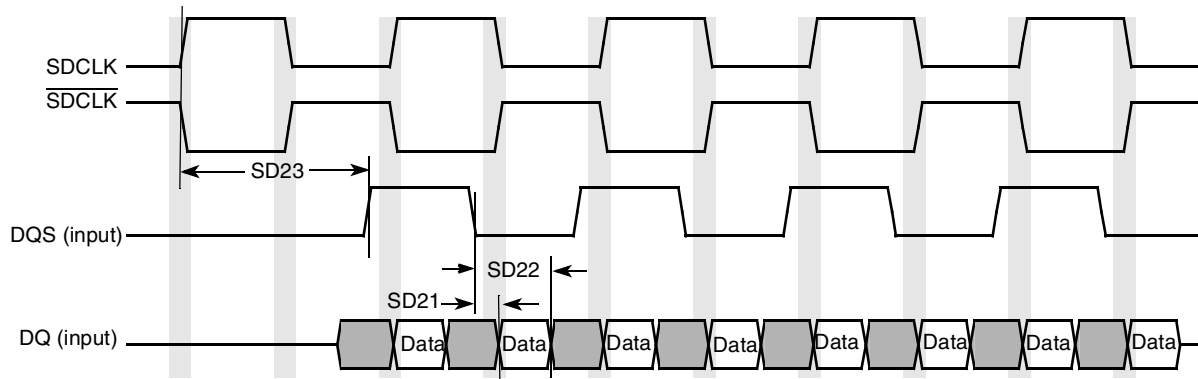


Figure 30. Mobile DDR SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 44. Mobile DDR SDRAM Read Cycle Timing Parameters

| ID | Parameter | Symbol | Min. | Max. | Unit |
|------|---|--------|------|------|------|
| SD21 | DQS – DQ Skew (defines the data valid window in read cycles related to DQS) | tDQSQ | — | 0.85 | ns |
| SD22 | DQS DQ HOLD time from DQS | tQH | 2.3 | — | ns |
| SD23 | DQS output access time from SDCLK posedge | tDQSCK | — | 6.7 | ns |

3.6.6.1.3 DDR2 SDRAM–Specific Parameters

The following diagrams and tables specify the timings related to the SDRAMC module which interfaces DDR2 SDRAM.

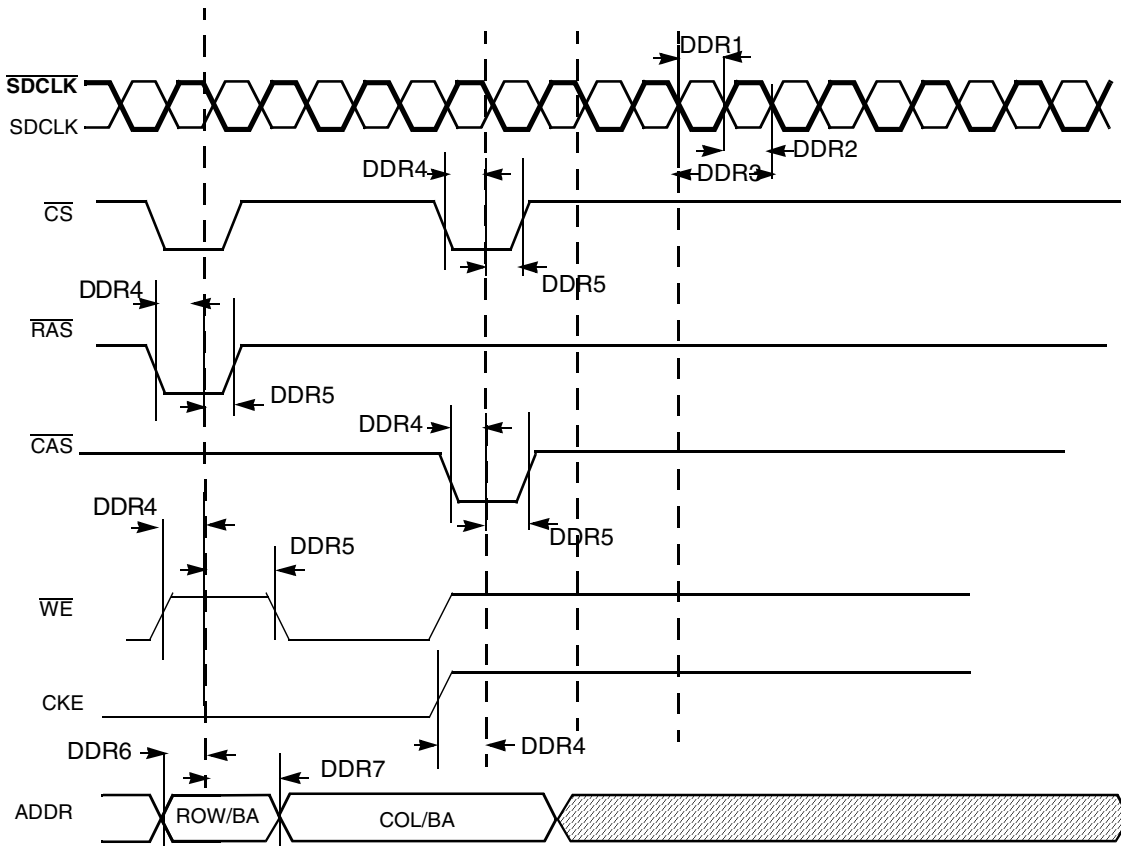


Figure 31. DDR2 SDRAM Basic Timing Parameters

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: i.MX25 Product Family

Table 45 provides values for a command/address slew rate of 1 V/ns and an SDCLK, SDCLK_B differential slew rate of 2 V/ns. For additional values, use Table 46, “tIS, tIH Derating Values for DDR2-400, DDR2-533.”

Table 45. DDR2 SDRAM Timing Parameter Table

| ID | Parameter | Symbol | DDR2-400 | | Unit |
|------|----------------------------------|--------|----------|------|------|
| | | | Min. | Max. | |
| DDR1 | SDRAM clock high-level width | tCH | 0.45 | 0.55 | tCK |
| DDR2 | SDRAM clock low-level width | tCL | 0.45 | 0.55 | tCK |
| DDR3 | SDRAM clock cycle time | tCK | 7.5 | 8 | ns |
| DDR4 | CS, RAS, CAS, CKE, WE setup time | tIS | 0.35 | — | ns |
| DDR5 | CS, RAS, CAS, CKE, WE hold time | tIH | 0.475 | — | ns |
| DDR6 | Address output setup time | tIS | 0.35 | — | ns |
| DDR7 | Address output hold time | tIH | 0.475 | — | ns |

Table 45 shows values for a command/address slew rate of 1 V/ns and an SDCLK, SDCLK_B differential slew rate of 2 V/ns. Table 46 shows additional values for DDR2-400 and DDR2-533.

Table 46. tIS, tIH Derating Values for DDR2-400, DDR2-533

| Command/ Address Slew Rate (V/Ns) | CK, CK Differential Slew Rate | | | | | | Units |
|---|-------------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-------|
| | 2.0 V/ns | | 1.5 V/ns | | 1.0 V/ns | | |
| | Δt_{IS} | Δt_{IH} | Δt_{IS} | Δt_{IH} | Δt_{IS} | Δt_{IH} | |
| 4.0 | +187 | +94 | +217 | +124 | +247 | +154 | ps |
| 3.5 | +179 | +89 | +209 | +119 | +239 | +149 | ps |
| 3.0 | +167 | +83 | +197 | +113 | +227 | +143 | ps |
| 2.5 | +150 | +75 | +180 | +105 | +210 | +135 | ps |
| 2.0 | +125 | +45 | +155 | +75 | +185 | +105 | ps |
| 1.5 | +83 | +21 | +113 | +51 | +143 | +81 | ps |
| 1.0 | 0 | 0 | +30 | +30 | +60 | +60 | ps |
| 0.9 | -11 | -14 | +19 | +16 | +49 | +46 | ps |
| 0.8 | -25 | -31 | +5 | -1 | +35 | +29 | ps |
| 0.7 | -43 | -54 | -13 | -24 | +17 | +6 | ps |
| 0.6 | -67 | -83 | -37 | -53 | -7 | -23 | ps |
| 0.5 | -110 | -125 | -80 | -95 | -50 | -65 | ps |
| 0.4 | -175 | -188 | -145 | -158 | -115 | -128 | ps |
| 0.3 | -285 | -292 | -255 | -262 | -225 | -232 | ps |
| 0.25 | -350 | -375 | -320 | -345 | -290 | -315 | ps |
| 0.2 | -525 | -500 | -495 | -470 | -465 | -440 | ps |
| 0.15 | -800 | -708 | -770 | -678 | -740 | -648 | ps |
| 0.1 | -1450 | -1125 | -1420 | -1095 | -1390 | -1065 | ps |

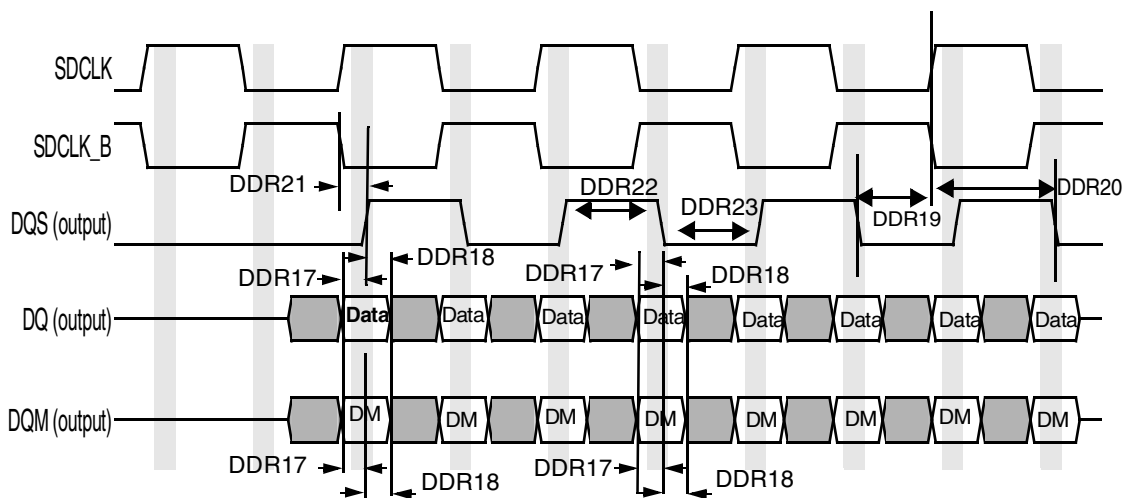


Figure 32. DDR2 SDRAM Write Cycle Timing Diagram

Table 47. DDR2 SDRAM Write Cycle Parameter Table

| ID | Parameter | Symbol | DDR2-400 | | Unit |
|-------|---|------------|----------|------|------|
| | | | Min. | Max. | |
| DDR17 | DQ & DQM setup time to DQS (single-ended strobe) ¹ | tDS1(base) | 0.025 | — | ns |
| DDR18 | DQ & DQM hold time to DQS (single-ended strobe) ¹ | tDH1(base) | 0.025 | — | ns |
| DDR19 | Write cycle DQS falling edge to SDCLK output setup time | tDSS | 0.2 | — | tCK |
| DDR20 | Write cycle DQS falling edge to SDCLK output hold time | tDSH | 0.2 | — | tCK |
| DDR21 | DQS latching rising transitions to associated clock edges | tDQSS | -0.25 | 0.25 | tCK |
| DDR22 | DQS high-level width | tDQSH | 0.35 | — | tCK |
| DDR23 | DQS low-level width | tDQSL | 0.35 | — | tCK |

¹ These values are for a DQ/DM slew rate of 1 V/ns and a DQS slew rate of 1 V/ns. For additional values use Table 48, “DtDS1, DtDH1 Derating Values for DDR2-400, DDR2-533.”

Table 48. ΔtDS1, ΔtDH1 Derating Values for DDR2-400, DDR2-533^{1,2,3}

| | | DQS Single-Ended Slew Rate | | | | | | | | | | | | | | | | | |
|----------------------|-----|----------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| | | 2.0 V/ns | | 1.5 V/ns | | 1.0 V/ns | | 0.9 V/ns | | 0.8 V/ns | | 0.7 V/ns | | 0.6 V/ns | | 0.5 V/ns | | 0.4 V/ns | |
| | | ΔtD S1 | ΔtD H1 | ΔtD S1 | ΔtD H1 | ΔtD S1 | ΔtD H1 | ΔtD S1 | ΔtD H1 | ΔtD S1 | ΔtD H1 | ΔtD S1 | ΔtD H1 | ΔtD S1 | ΔtD H1 | ΔtD S1 | ΔtD H1 | ΔtD S1 | ΔtD H1 |
| DQ Slew Rate V/ns | 2.0 | 188 | 188 | 167 | 146 | 125 | 63 | — | — | — | — | — | — | — | — | — | — | — | — |
| | 1.5 | 146 | 167 | 125 | 125 | 83 | 42 | 81 | 43 | — | — | — | — | — | — | — | — | — | — |
| | 1.0 | 63 | 125 | 42 | 83 | 0 | 0 | -2 | 1 | -7 | -13 | — | — | — | — | — | — | — | — |
| | 0.9 | — | — | 31 | 69 | -11 | -14 | -13 | -13 | -18 | -27 | -29 | -45 | — | — | — | — | — | — |
| | 0.8 | — | — | — | — | -25 | -31 | -27 | -30 | -32 | -44 | -43 | -62 | -60 | -86 | — | — | — | — |
| | 0.7 | — | — | — | — | — | — | -45 | -53 | -50 | -67 | -61 | -85 | -78 | -109 | -108 | -152 | — | — |
| | 0.6 | — | — | — | — | — | — | — | — | -74 | -96 | -85 | -114 | -102 | -138 | -132 | -181 | -183 | -246 |
| | 0.5 | — | — | — | — | — | — | — | — | — | — | -128 | -156 | -145 | -180 | -175 | -223 | -226 | -288 |
| | 0.4 | — | — | — | — | — | — | — | — | — | — | — | — | -210 | -243 | -240 | -286 | -291 | -351 |

¹ All units in ‘ps’.

² Test conditions are at capacitance=15pF for DDR PADS. Recommended drive strengths are medium for SDCLK and high for address and controls.

³ SDRAM CLK and DQS related parameters are measured from the 50% point. That is, high is defined as 50% of the signal value, and low is defined as 50% of the signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and SDCLK (inverted clock).

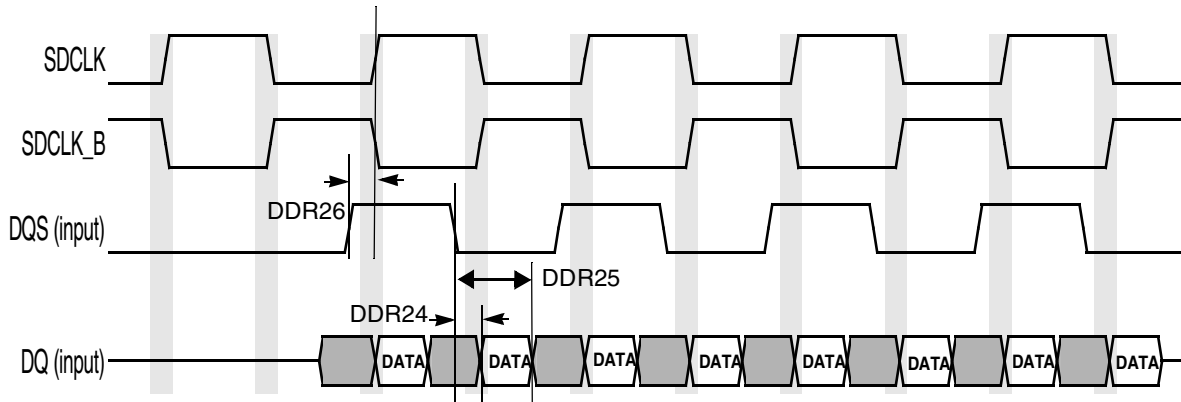


Figure 33. DDR2 SDRAM DQ vs. DQS and SDCLK READ Cycle Timing Diagram

Table 49. DDR2 SDRAM Read Cycle Parameter Table^{1,2}

| ID | Parameter | Symbol | DDR2-400 | | Unit |
|-------|---|--------|----------|------|------|
| | | | Min. | Max. | |
| DDR24 | DQS - DQ Skew (defines the Data valid window in read cycles related to DQS) | tdQSQ | — | 0.35 | ns |
| DDR25 | DQS DQ in HOLD time from DQS ³ | tQH | 2.925 | — | ns |
| DDR26 | DQS output access time from SDCLK posedge | tdQSCK | -0.5 | 0.5 | ns |

¹ Test conditions are at capacitance=15 pF for DDR PADS. Recommended drive strengths are medium for SDCLK and high for address and controls.

² SDRAM CLK and DQS-related parameters are measured from the 50% point. That is, high is defined as 50% of the signal value, and low is defined as 50% of the signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and SDCLK (inverted clock).

³ The value was calculated for an SDCLK frequency of 133 MHz, by the formula $tQH = tHP - tQHS = \min(tCL, tCH) - tQHS = 0.45 \cdot tCK - tQHS = 0.45 \cdot 7.5 - 0.45 = 2.925 \text{ ns}$

3.6.6.2 NAND Flash Controller (NFC) Timing

The i.MX25 NFC supports normal timing mode, using two Flash clock cycles for one access of \overline{RE} and \overline{WE} . AC timings are provided as multiplications of the clock cycle and fixed delay. [Figure 34](#) through [Figure 37](#) depicts the relative timing between NFC signals at the module level for different operations under normal mode. [Table 50](#) describes the timing parameters (NF1–NF17) that are shown in the figures.

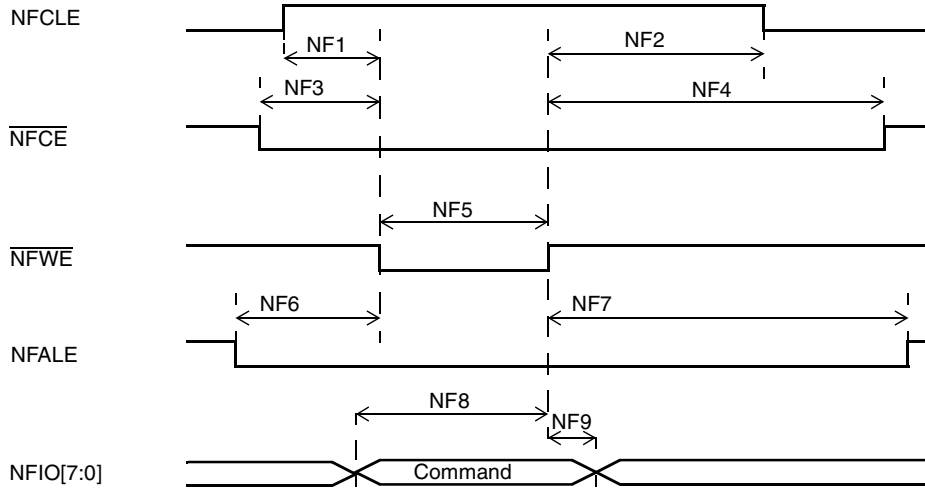


Figure 34. Command Latch Cycle Timing Diagram

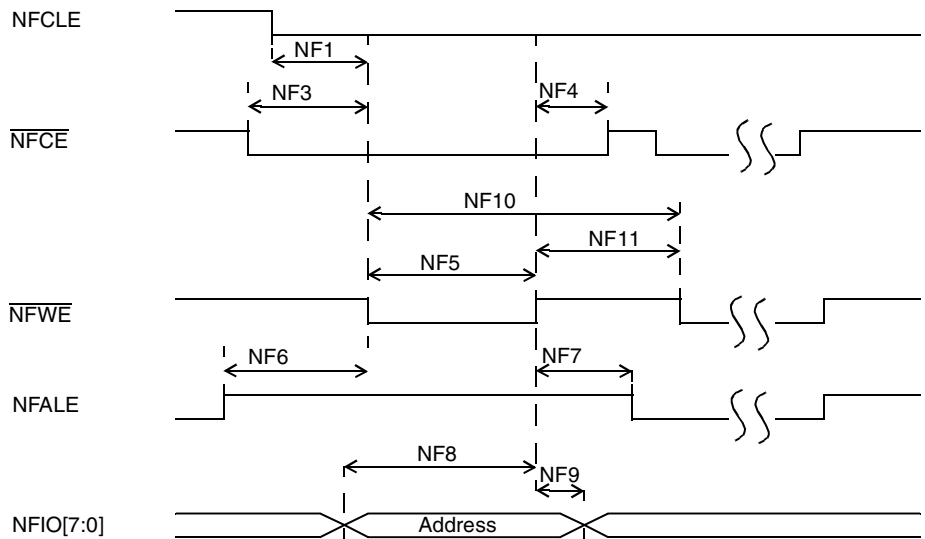


Figure 35. Address Latch Cycle Timing Diagram

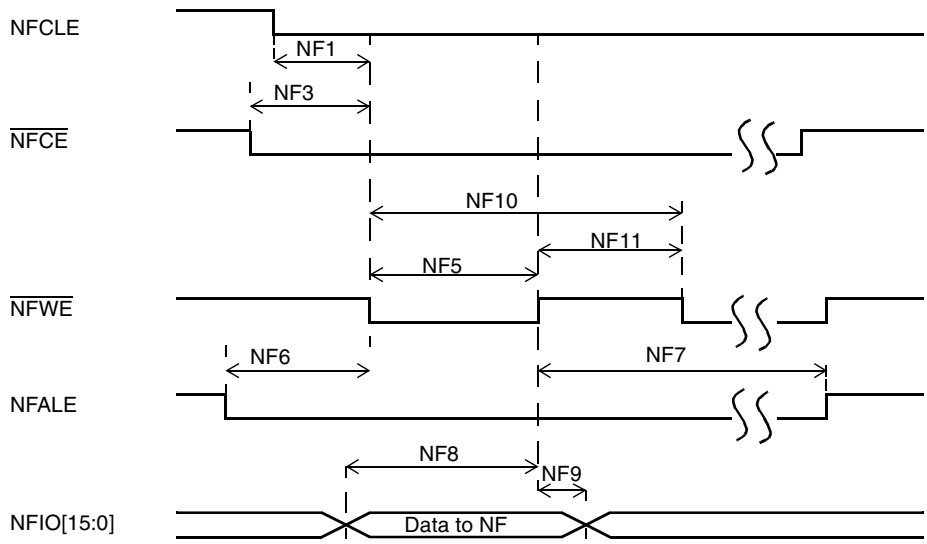


Figure 36. Write Data Latch Cycle Timing Diagram

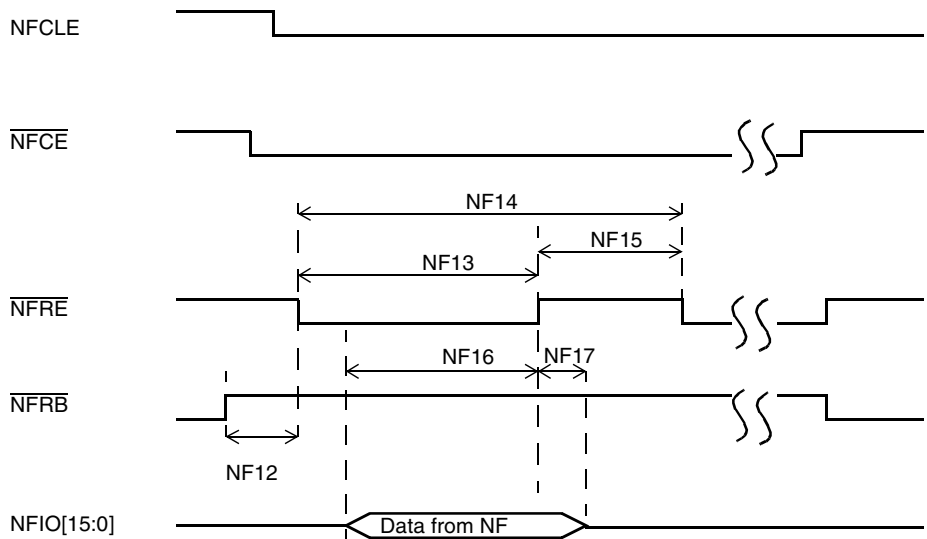


Figure 37. Read Data Latch Cycle Timing Diagram

Table 50. NFC Timing Parameters¹

| ID | Parameter | Symbol | Timing T = NFC Clock Cycle | | Example Timing for NFC Clock ≈ 33 MHz T = 30 ns | | Unit |
|-----|------------------|--------|-------------------------------|------|---|------|------|
| | | | Min. | Max. | Min. | Max. | |
| NF1 | NFCLE setup time | tCLS | T-1.0 ns | — | 29 | — | ns |
| NF2 | NFCLE hold time | tCLH | T-2.0 ns | — | 28 | — | ns |
| NF3 | NFCE setup time | tCS | T-1.0 ns | — | 29 | — | ns |
| NF4 | NFCE hold time | tCH | T-2.0 ns | — | 28 | — | ns |

Table 50. NFC Timing Parameters¹ (continued)

| ID | Parameter | Symbol | Timing T = NFC Clock Cycle | | Example Timing for NFC Clock ≈ 33 MHz T = 30 ns | | Unit |
|------|---|--------|-------------------------------|------|---|------|------|
| | | | Min. | Max. | Min. | Max. | |
| NF5 | $\overline{\text{NF_WP}}$ pulse width | tWP | T–1.5 ns | | 28.5 | | ns |
| NF6 | NFALE setup time | tALS | T | — | 30 | — | ns |
| NF7 | NFALE hold time | tALH | T–3.0 ns | — | 27 | — | ns |
| NF8 | Data setup time | tDS | T | — | 30 | — | ns |
| NF9 | Data hold time | tDH | T–5.0 ns | — | 25 | — | ns |
| NF10 | Write cycle time | tWC | 2T | | 60 | | ns |
| NF11 | $\overline{\text{NFWE}}$ hold time | tWH | T–2.5 ns | | 27.5 | | ns |
| NF12 | Ready to $\overline{\text{NFRE}}$ low | tRR | 6T | — | 180 | — | ns |
| NF13 | $\overline{\text{NFRE}}$ pulse width | tRP | 1.5T | — | 45 | — | ns |
| NF14 | READ cycle time | tRC | 2T | — | 60 | — | ns |
| NF15 | $\overline{\text{NFRE}}$ high hold time | tREH | 0.5T–2.5 ns | | 12.5 | — | ns |
| NF16 | Data setup on read | tDSR | N/A | | 10 | — | ns |
| NF17 | Data hold on read | tDHR | N/A | | 0 | — | ns |

¹ The Flash clock maximum frequency is 50 MHz.

NOTE

For timing purposes, transition to signal high is defined as 80% of signal value; while signal low is defined as 20% of signal value.

Timing for HCLK is 133 MHz. The internal NFC clock (Flash clock) is approximately 33 MHz (30 ns). All timings are listed according to this NFC clock frequency (multiples of NFC clock phases), except NF16 and NF17, which are not related to the NFC clock.

3.6.6.3 Wireless External Interface Module (WEIM) Timing

Figure 38 depicts the timing of the WEIM module, and Table 51 describes the timing parameters (WE1–WE27) shown in the figure.

All WEIM output control signals may be asserted and negated by internal clock relative to BCLK rising edge or falling edge according to corresponding assertion/negation control fields. Address always begins relative to BCLK falling edge, but may be ended on rising or falling edge in muxed mode according to the control register configuration. Output data begins relative to BCLK rising edge except in muxed mode, where rising or falling edge may be used according to the control register configuration. Input data, $\overline{\text{ECB}}$ and $\overline{\text{DTACK}}$ are all captured relative to BCLK rising edge.

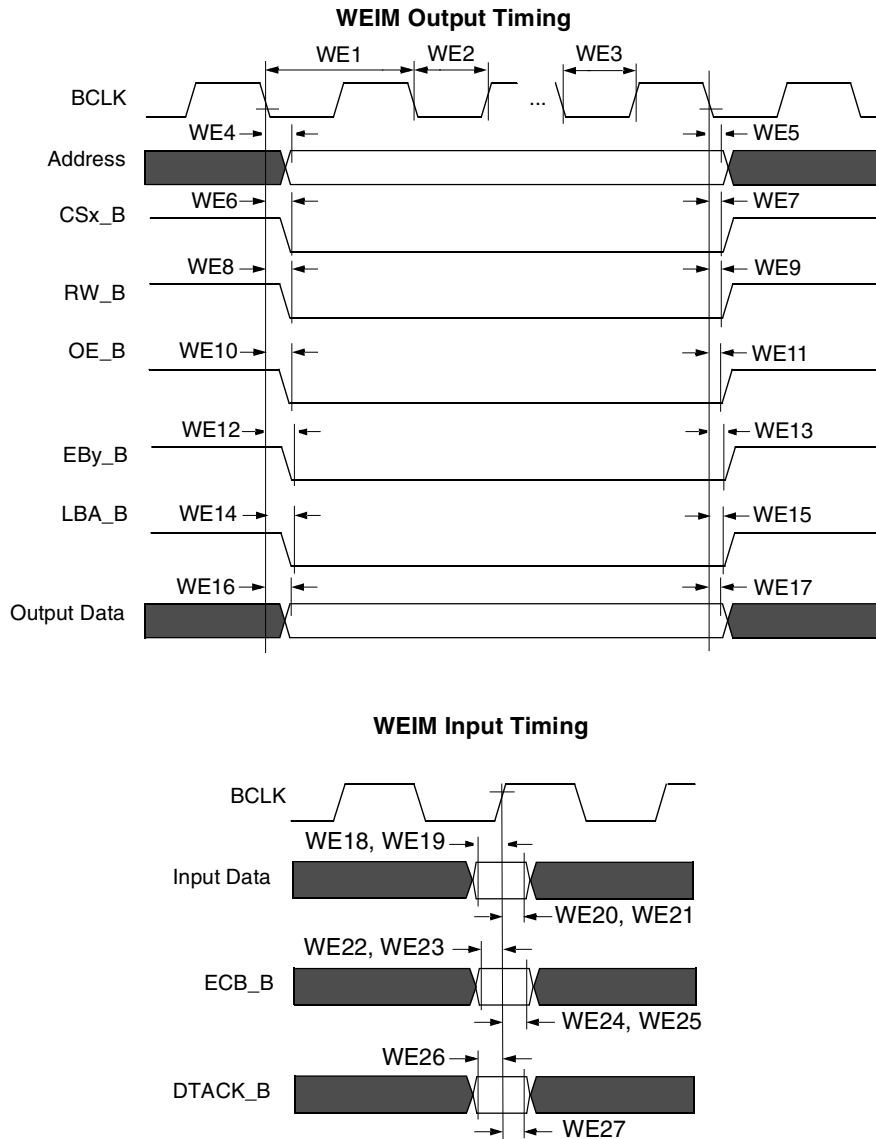


Figure 38. WEIM Bus Timing Diagram

Table 51. WEIM Bus Timing Parameters¹

| ID | Parameter | Min. | Max. | Unit |
|-----|------------------------------------|------|------|------|
| WE1 | BCLK cycle time ² | 7.5 | — | ns |
| WE2 | BCLK low-level width ² | 3.0 | — | ns |
| WE3 | BCLK high-level width ² | 3.0 | — | ns |
| WE4 | Clock fall to address valid | 0.7 | 2.0 | ns |
| WE5 | Clock rise/fall to address invalid | 0.7 | 2.5 | ns |
| WE6 | Clock rise/fall to CSx_B valid | 0.4 | 2.3 | ns |
| WE7 | Clock rise/fall to CSx_B invalid | 0.4 | 2.3 | ns |

Table 51. WEIM Bus Timing Parameters¹ (continued)

| ID | Parameter | Min. | Max. | Unit |
|------|---|------|------|------|
| WE8 | Clock rise/fall to RW_B valid | 0.9 | 2.6 | ns |
| WE9 | Clock rise/fall to RW_B invalid | 0.9 | 2.6 | ns |
| WE10 | Clock rise/fall to OE_B valid | 1.2 | 2.5 | ns |
| WE11 | Clock rise/fall to OE_B invalid | 1.2 | 2.5 | ns |
| WE12 | Clock rise/fall to EBy_B valid | 0.7 | 2.4 | ns |
| WE13 | Clock rise/fall to EBy_B invalid | 0.7 | 2.4 | ns |
| WE14 | Clock rise/fall to LBA_B valid | 1.0 | 2.8 | ns |
| WE15 | Clock rise/fall to LBA_B invalid | 1.0 | 2.8 | ns |
| WE16 | Clock rise/fall to output data valid | 1.0 | 3.0 | ns |
| WE17 | Clock rise to output data invalid | 1.0 | 3.0 | ns |
| WE18 | Input data valid to clock rise, FCE=1 | 1.2 | — | ns |
| WE19 | Input data valid to clock rise, FCE=0 | 6.9 | — | ns |
| WE20 | Clock rise to input data invalid, FCE=1 | 0.2 | — | ns |
| WE21 | Clock rise to input data invalid, FCE=0 | 2.4 | — | ns |
| WE22 | ECB_B setup time, FCE=1 | 1.1 | — | ns |
| WE23 | ECB_B setup time, FCE=0 | 7.2 | — | ns |
| WE24 | ECB_B hold time, FCE=1 | 0 | — | ns |
| WE25 | ECB_B hold time, FCE=0 | 0 | — | ns |
| WE26 | DTACK_B setup time | 5.4 | — | ns |
| WE27 | DTACK_B hold time | -3.2 | — | ns |

¹ High is defined as 80% of signal value; low is defined as 20% of signal value.

² BCLK parameters are being measured from the 50% point. For example, high is defined as 50% of signal value and low is defined as 50% as signal value.

NOTE

The test condition load capacitance was 25 pF. Recommended drive strength for all controls, address, and BCLK is maximum drive.

Recommended drive strength for all controls, address and BCLK is maximum drive.

Figure 39 through Figure 44 give examples of basic WEIM accesses to external memory devices with the timing parameters described in Table 51 for specific control parameter settings.

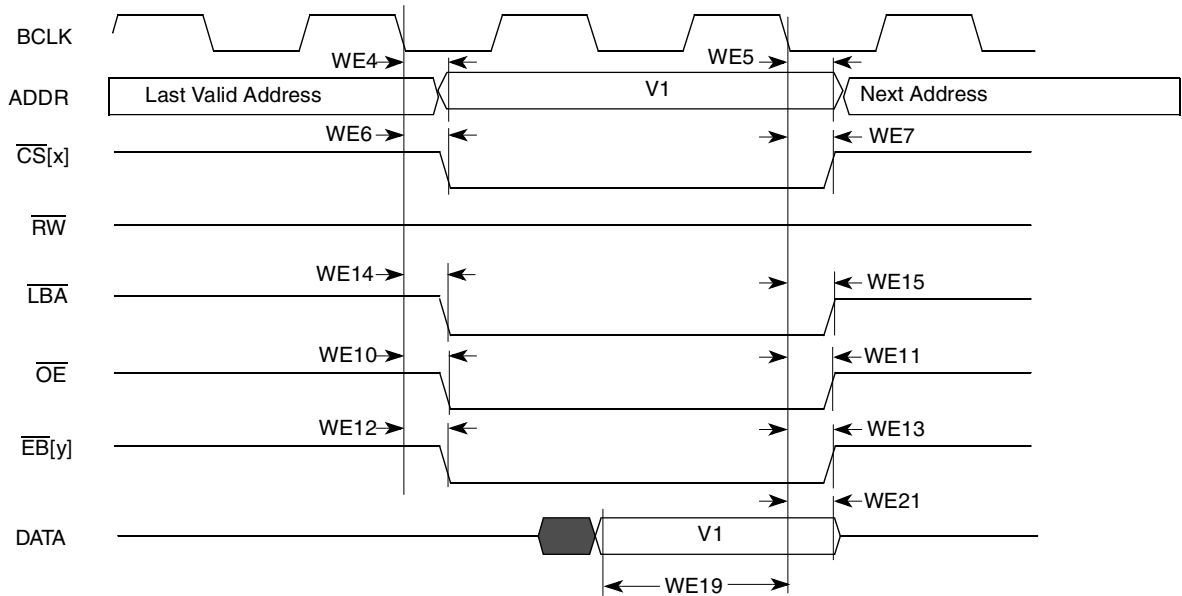


Figure 39. Synchronous Memory Timing Diagram for Read Access—WSC=1

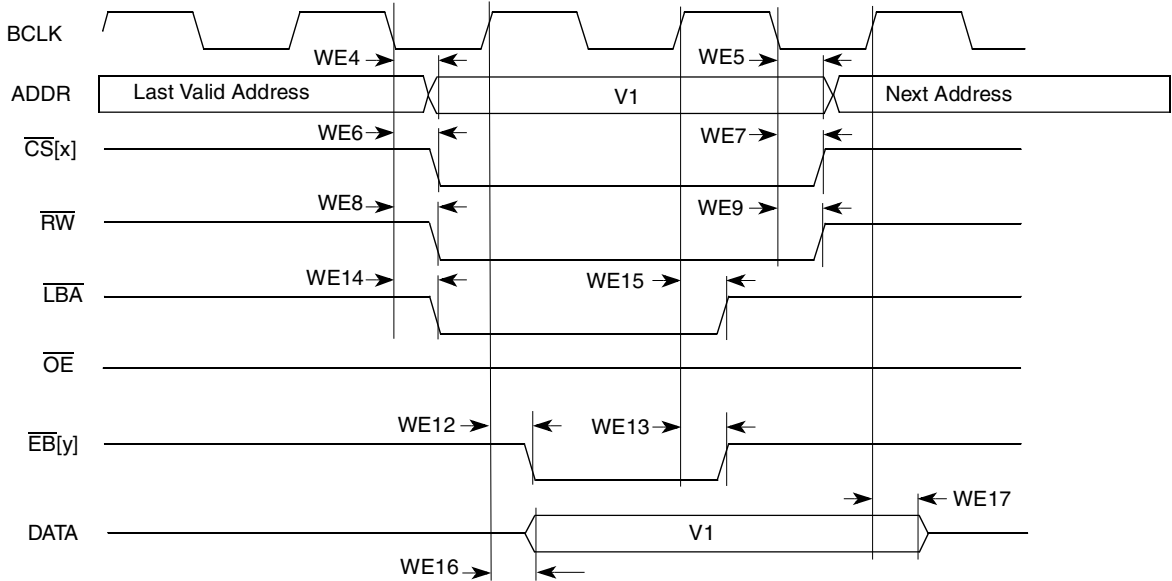
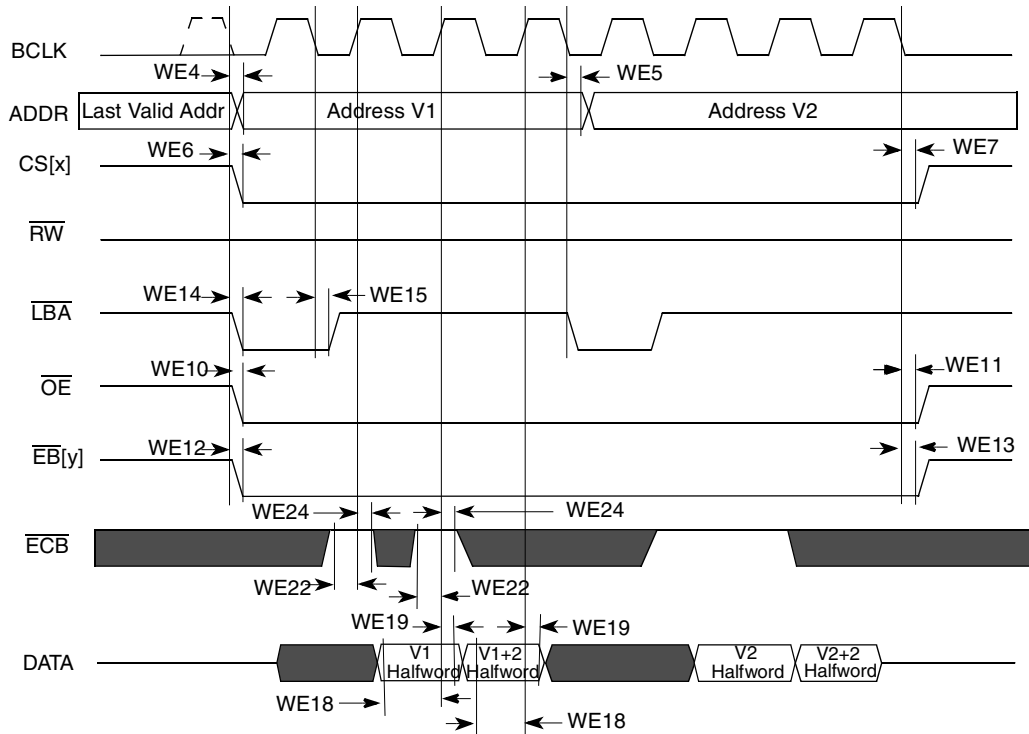
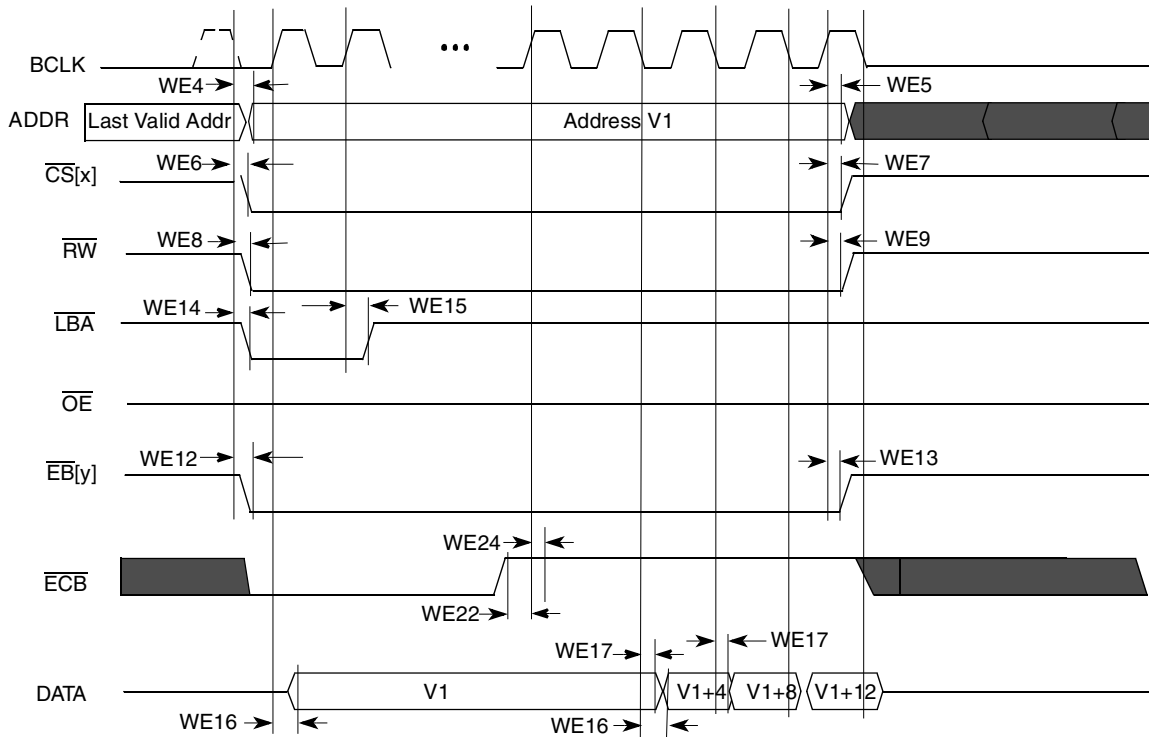


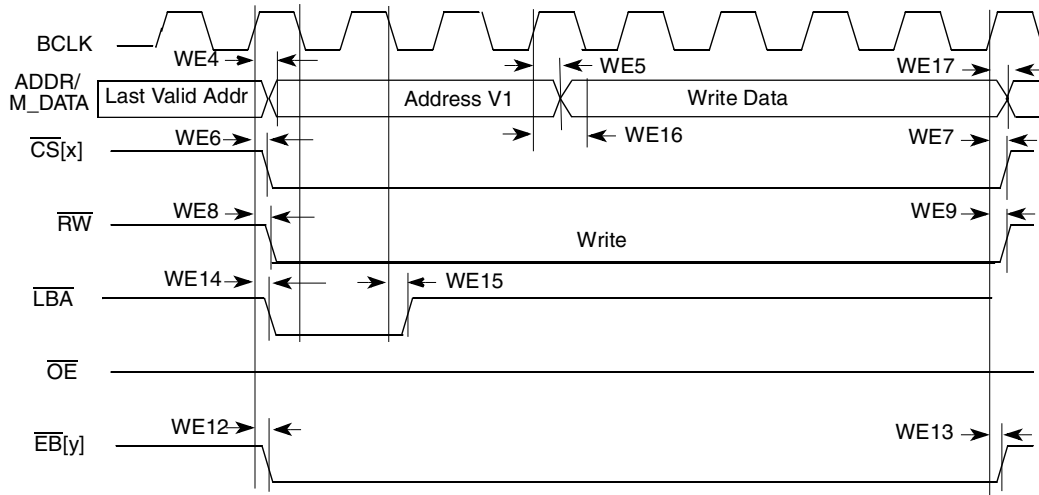
Figure 40. Synchronous Memory Timing Diagram for Write Access—WSC=1, EBWA=1, EBWN=1, LBN=1



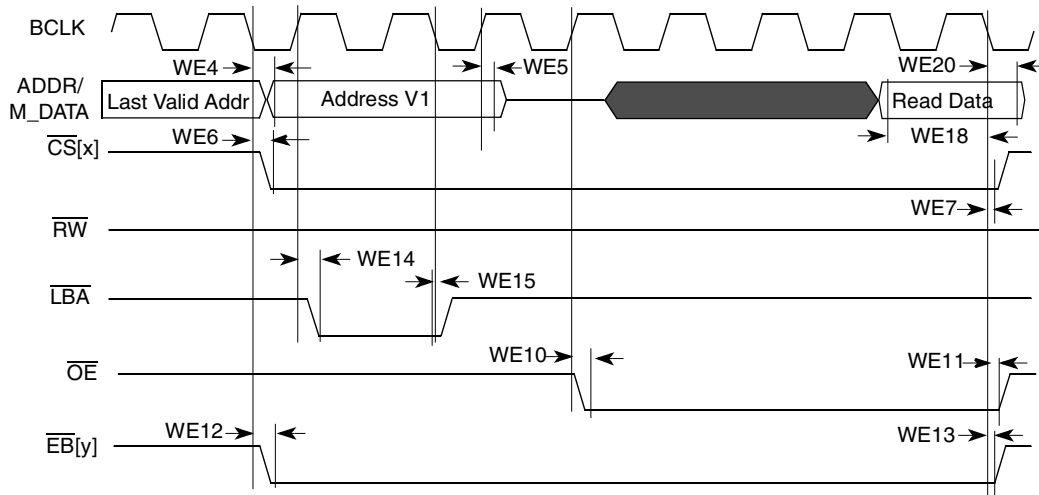
**Figure 41. Synchronous Memory Timing Diagram for Two Non-Sequential Read Accesses—
WSC=2, SYNC=1, DOL=0**



**Figure 42. Synchronous Memory Timing Diagram for Burst Write Access—
BCS=1, WSC=4, SYNC=1, DOL=0, PSR=1**



**Figure 43. Muxed A/D Mode Timing Diagram for Synchronous Write Access—
WSC=7, LBA=1, LBN=1, LAH=1**



**Figure 44. Muxed A/D Mode Timing Diagram for Synchronous Read Access—
WSC=7, LBA=1, LBN=1, LAH=1, OEA=7**

Figure 45 through Figure 49, and Table 49 help to determine timing parameters relative chip select (CS) state for asynchronous and DTACK WEIM accesses with corresponding WEIM bit fields and the timing parameters mentioned above.

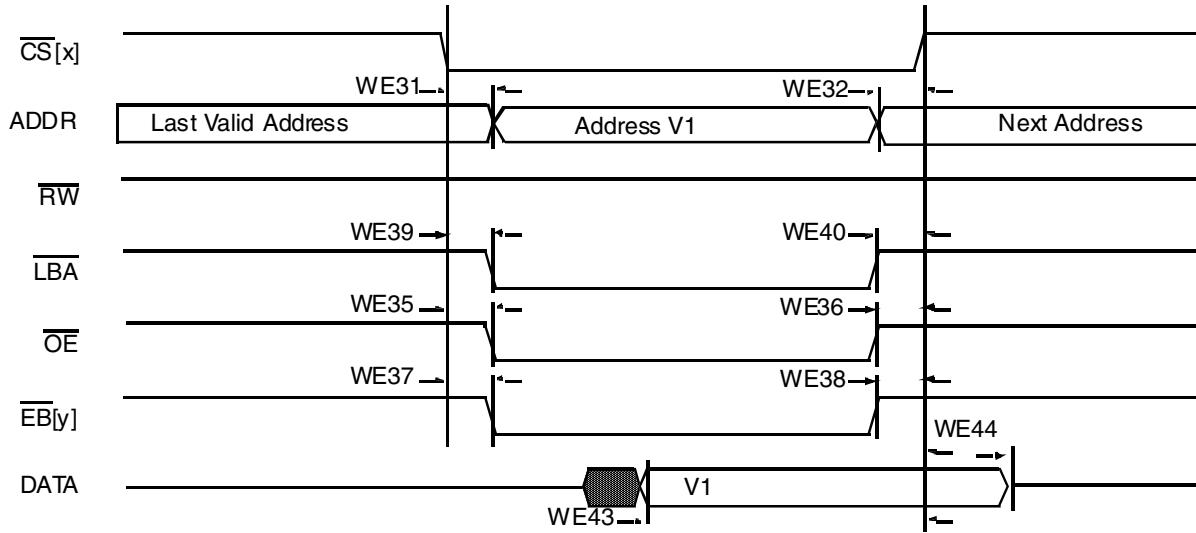


Figure 45. Asynchronous Memory Read Access

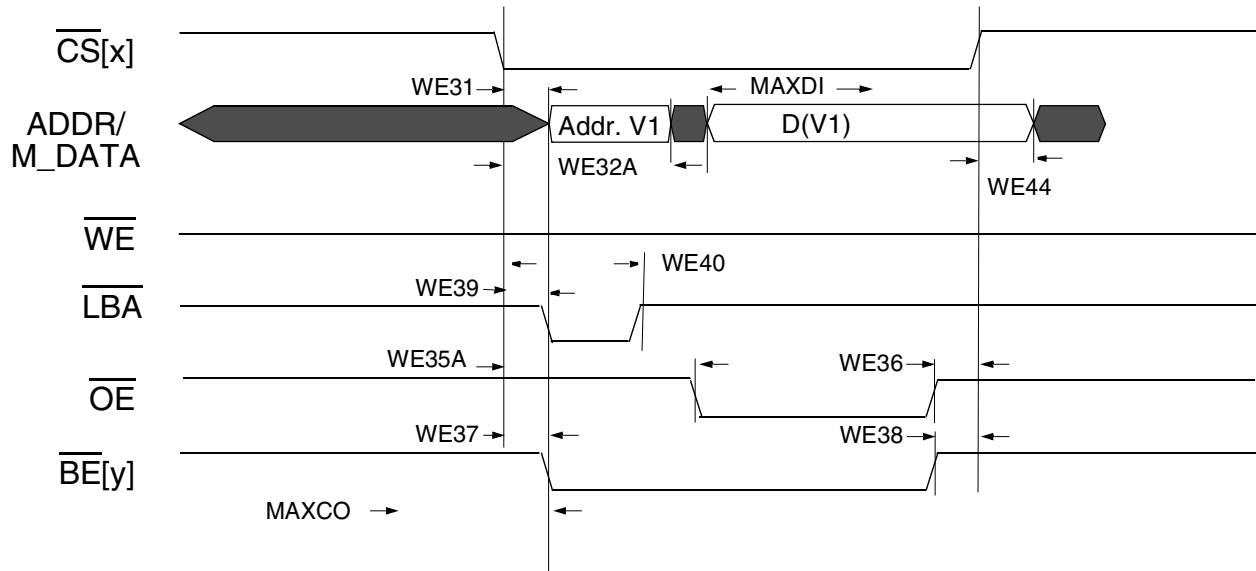


Figure 46. Asynchronous A/D Mixed Read Access (RWSC = 5)

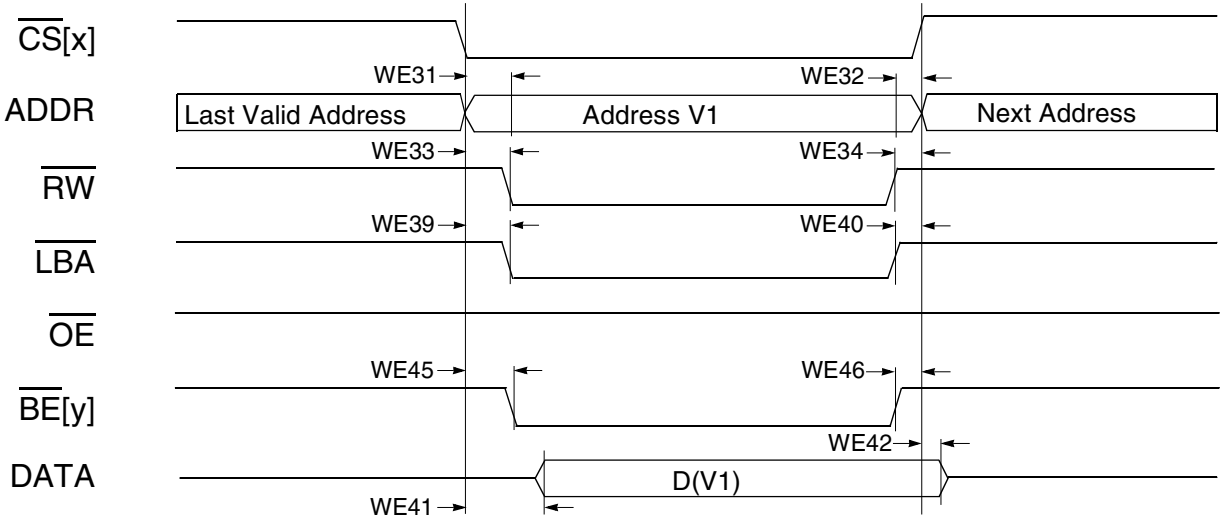


Figure 47. Asynchronous Memory Write Access

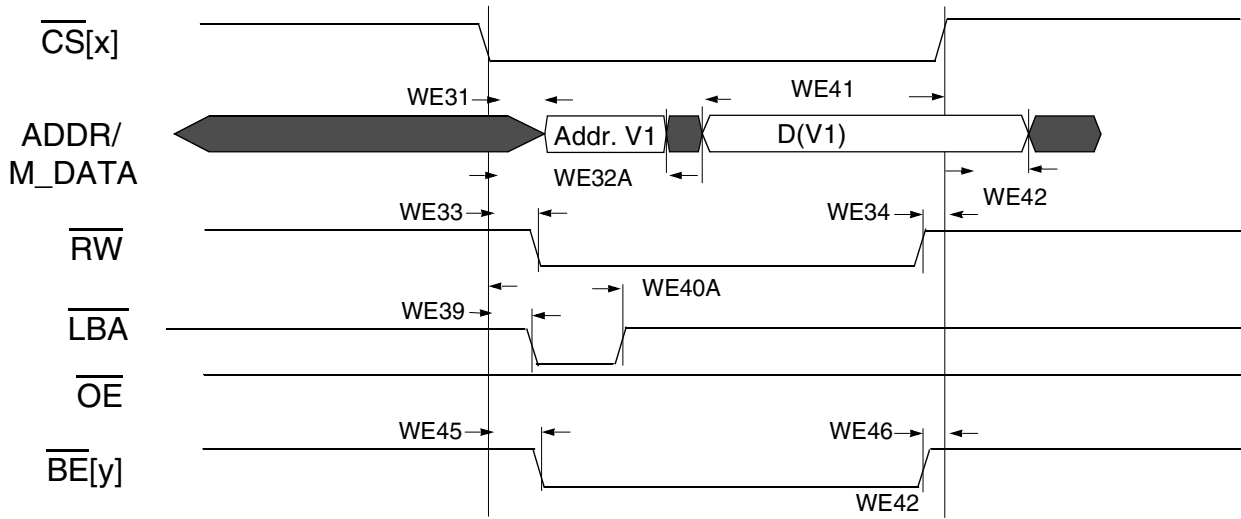


Figure 48. Asynchronous A/D Mux Write Access

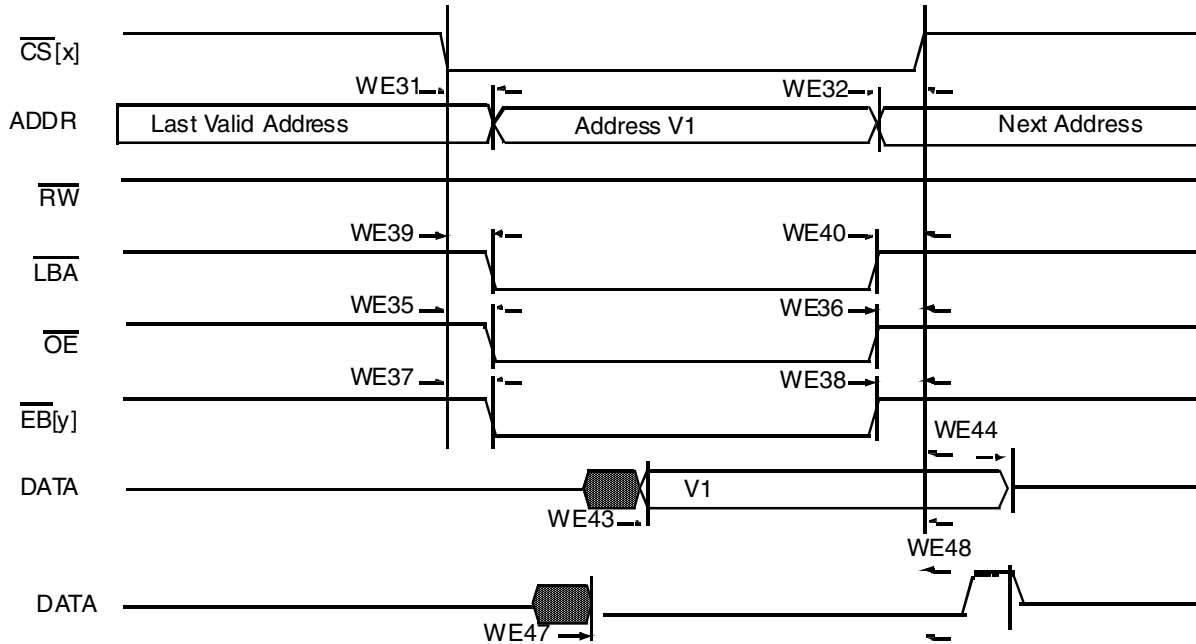


Figure 49. DTACK Read Access

Table 52. WEIM Asynchronous Timing Parameters Relative Chip Select Table

| Ref No. | Parameter | Determination By Synchronous Measured Parameters ¹ | Min | Max (If 133 MHz is supported by SoC) | Unit |
|-------------------|--|---|--|---|------|
| WE31 | $\overline{CS}[x]$ valid to Address Valid | $WE4 - WE6 - CSA^2$ | — | $3 - CSA$ | ns |
| WE32 | Address Invalid to $\overline{CS}[x]$ invalid | $WE7 - WE5 - CSN^3$ | — | $3 - CSN$ | ns |
| WE32A (muxed A/D) | $\overline{CS}[x]$ valid to Address Invalid | $WE4 - WE7 + (LBN + LBA + 1 - CSA^2)$ | $-3 + (LBN + LBA + 1 - CSA)$ | — | ns |
| WE33 | $\overline{CS}[x]$ Valid to \overline{WE} Valid | $WE8 - WE6 + (WEA - CSA)$ | — | $3 + (WEA - CSA)$ | ns |
| WE34 | \overline{WE} Invalid to $\overline{CS}[x]$ Invalid | $WE7 - WE9 + (WEN - CSN)$ | — | $3 - (WEN_CSN)$ | ns |
| WE35 | $\overline{CS}[x]$ Valid to \overline{OE} Valid | $WE10 - WE6 + (OEA - CSA)$ | — | $3 + (OEA - CSA)$ | ns |
| WE35A (muxed A/D) | $\overline{CS}[x]$ Valid to \overline{OE} Valid | $WE10 - WE6 + (OEA + RLBN + RLBA + ADH + 1 - CSA)$ | $-3 + (OEA + RLBN + RLBA + ADH + 1 - CSA)$ | $3 + (OEA + RLBN + RLBA + ADH + 1 - CSA)$ | ns |
| WE36 | \overline{OE} Invalid to $\overline{CS}[x]$ Invalid | $WE7 - WE11 + (OEN - CSN)$ | — | $3 - (OEN - CSN)$ | ns |
| WE37 | $\overline{CS}[x]$ Valid to $\overline{BE}[y]$ Valid (Read access) | $WE12 - WE6 + (RBEA - CSA)$ | — | $3 + (RBEA^4 - CSA)$ | ns |
| WE38 | $\overline{BE}[y]$ Invalid to $\overline{CS}[x]$ Invalid (Read access) | $WE7 - WE13 + (RBEN - CSN)$ | — | $3 - (RBEN^5 - CSN)$ | ns |
| WE39 | $\overline{CS}[x]$ Valid to \overline{LBA} Valid | $WE14 - WE6 + (LBA - CSA)$ | — | $3 + (LBA - CSA)$ | ns |
| WE40 | \overline{LBA} Invalid to $\overline{CS}[x]$ Invalid | $WE7 - WE15 - CSN$ | — | $3 - CSN$ | ns |

Table 52. WEIM Asynchronous Timing Parameters Relative Chip Select Table (continued)

| Ref No. | Parameter | Determination By Synchronous Measured Parameters ¹ | Min | Max (If 133 MHz is supported by SoC) | Unit |
|-------------------|---|---|--|--------------------------------------|------|
| WE40A (muxed A/D) | $\overline{CS}[x]$ Valid to \overline{LBA} Invalid | $WE14 - WE6 + (LBN + LBA + 1 - CSA)$ | $-3 + (LBN + LBA + 1 - CSA)$ | $3 + (LBN + LBA + 1 - CSA)$ | ns |
| WE41 | $\overline{CS}[x]$ Valid to Output Data Valid | $WE16 - WE6 - WCSA$ | — | $3 - WCSA$ | ns |
| WE41A (muxed A/D) | $\overline{CS}[x]$ Valid to Output Data Valid | $WE16 - WE6 + (WLBN + WLBA + ADH + 1 - WCSA)$ | — | $3 + (WLBN + WLBA + ADH + 1 - WCSA)$ | ns |
| WE42 | Output Data Invalid to $\overline{CS}[x]$ Invalid | $WE17 - WE7 - CSN$ | — | $3 - CSN$ | ns |
| WE43 | Input Data Valid to $\overline{CS}[x]$ Invalid | $MAXCO - MAXCSO + MAXDI$ | $MAXCO^6 - MAXCSO^7 + MAXDI^8$ | — | ns |
| WE44 | $\overline{CS}[x]$ Invalid to Input Data invalid | 0 | 0 | — | ns |
| WE45 | $\overline{CS}[x]$ Valid to $\overline{BE}[y]$ Valid (Write access) | $WE12 - WE6 + (WBEA - CSA)$ | — | $3 + (WBEA - CSA)$ | ns |
| WE46 | $\overline{BE}[y]$ Invalid to $\overline{CS}[x]$ Invalid (Write access) | $WE7 - WE13 + (WBEN - CSN)$ | — | $-3 + (WBEN - CSN)$ | ns |
| WE47 | \overline{DTACK} Valid to $\overline{CS}[x]$ Invalid | $MAXCO - MAXCSO + MAXDTI$ | $MAXCO^6 - MAXCSO^7$ Note: Note: $e: + MAXDTI^9$ | — | ns |
| WE48 | $\overline{CS}[x]$ Invalid to \overline{DTACK} invalid | 0 | 0 | — | ns |

¹ For the value of parameters WE4–WE21, see column BCD = 0 in Table 51.

² \overline{CS} Assertion. This bit field determines when the \overline{CS} signal is asserted during read/write cycles.

³ \overline{CS} Negation. This bit field determines when the \overline{CS} signal is negated during read/write cycles.

⁴ \overline{BE} Assertion. This bit field determines when the \overline{BE} signal is asserted during read cycles.

⁵ \overline{BE} Negation. This bit field determines when the \overline{BE} signal is negated during read cycles.

⁶ Output maximum delay from internal driving ADDR/control FFs to chip outputs.

⁷ Output maximum delay from $\overline{CS}[x]$ internal driving FFs to $\overline{CS}[x]$ out.

⁸ DATA maximum delay from chip input data to its internal FF.

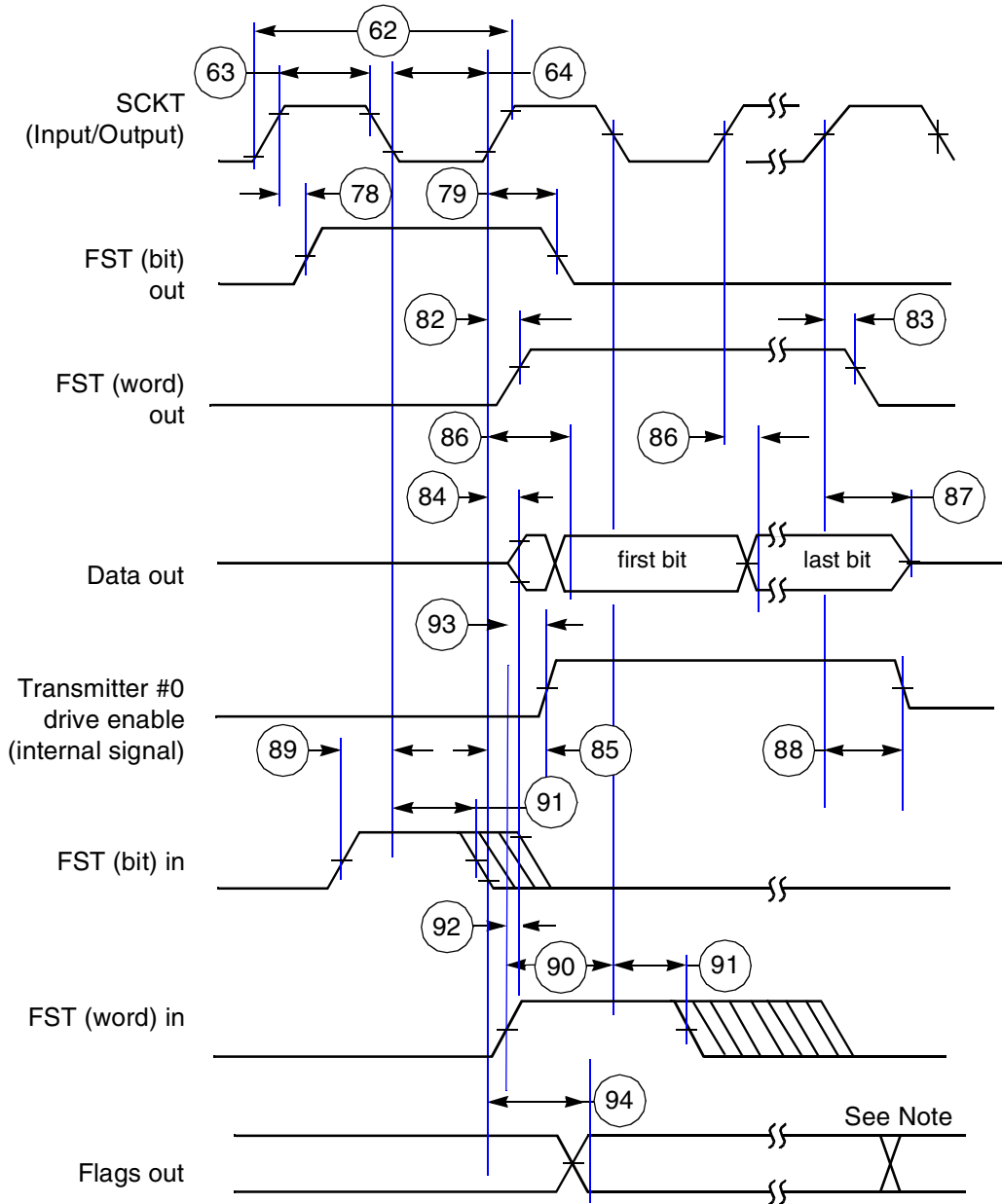
⁹ DTACK maximum delay from chip dtack input to its internal FF.

Note: All configuration parameters (CSA,CSN,WBEA,WBEN,LBA,LBN,OEN,OEA,RBEA & RBEN) are in cycle units.

3.6.7 Enhanced Serial Audio Interface (ESAI) Timing

This section describes general timing requirements for ESAI, as well as the ESAI transmit and receive timing.

Figure 50 shows the ESAI transmit timing diagram.



Note: In network mode, output flag transitions can occur at the start of each time slot within the frame. In normal mode, the output flag state is asserted for the entire frame period.

Figure 50. ESAI Transmit Timing

Figure 51 shows the ESAI receive timing diagram.

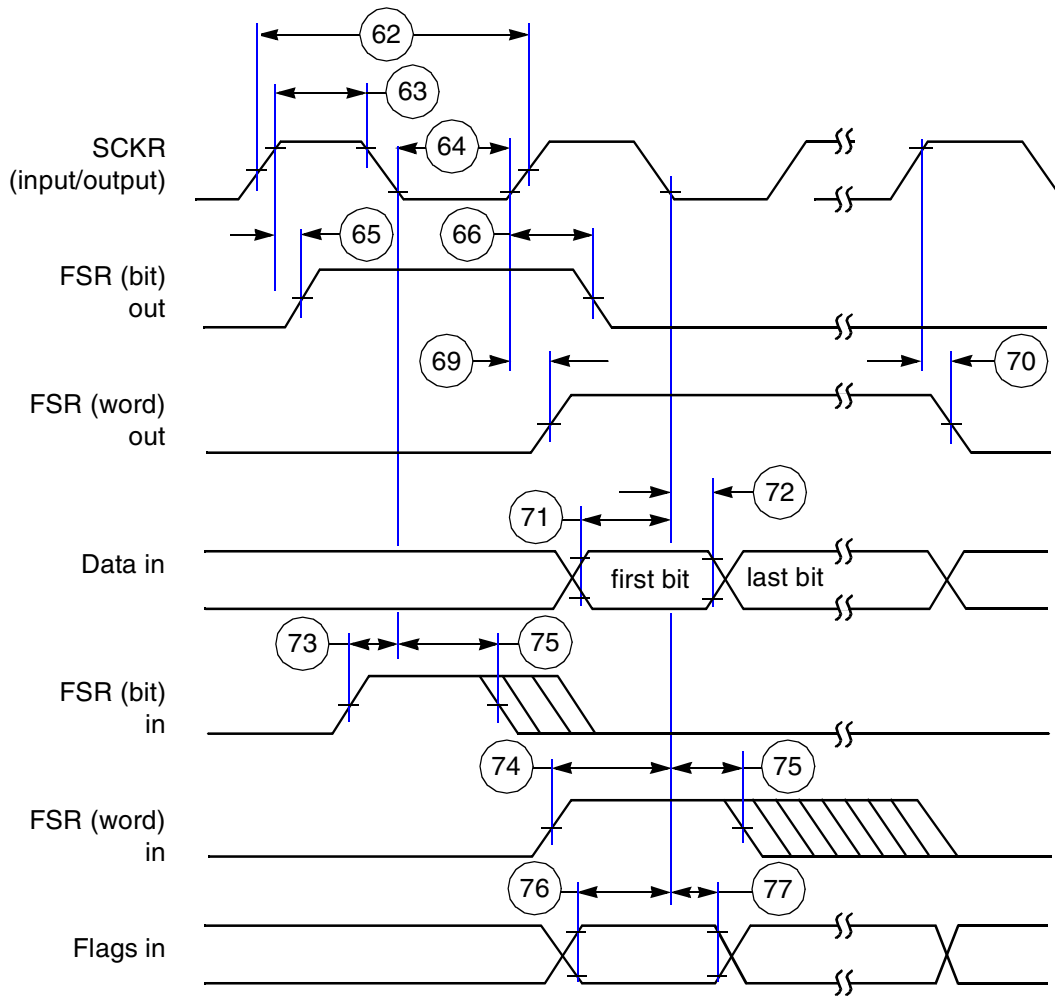


Figure 51. ESAI Receive Timing Diagram

Figure 52 shows the ESAI HCKT timing diagram.

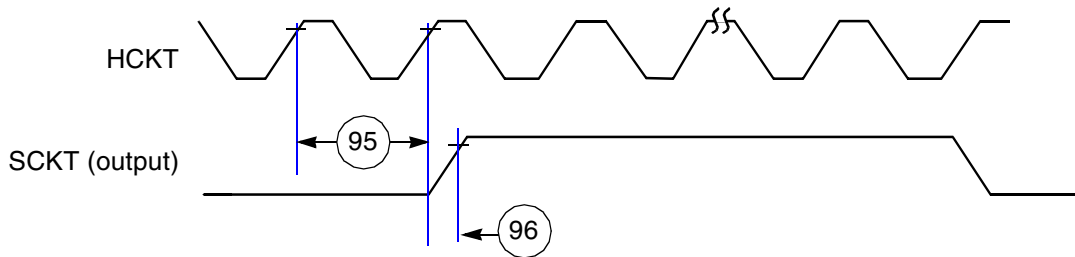


Figure 52. ESAI HCKT Timing

Figure 53 shows the ESAI HCKR timing diagram.

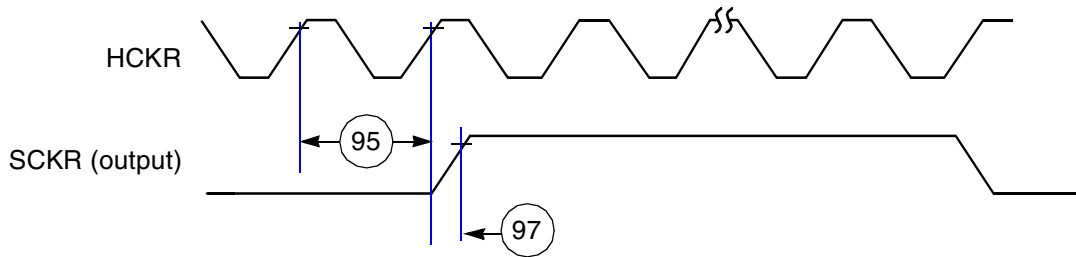


Figure 53. ESAI HCKR Timing

Table 55 describes the general timing requirements for the ESAI module. Table 53 and Table 54 describe respectively the conditions and signals cited in Table 55.

Table 53. ESAI Timing Conditions

| Symbol | Significance | Comments |
|--------|-----------------------------------|--|
| i ck | Internal clock | In the i.MX25, the internal clock frequency is equal to the IP bus frequency (133 MHz) |
| x ck | External clock | The external clock may be derived from the CRM module or other external clock sources |
| i ck a | Internal clock, asynchronous mode | In asynchronous mode, SCKT and SCKR are different clocks |
| i ck s | Internal clock, synchronous mode | In synchronous mode, SCKT and SCKR are the same clock |

Table 54. ESAI Signals

| Signal Name | Significance |
|-------------|-------------------------------|
| SCKT | Transmit clock |
| SCKR | Receive clock |
| FST | Transmit frame sync |
| HCKT | Transmit high-frequency clock |
| HCKR | Receive high-frequency clock |

Table 55. ESAI General Timing Requirements

| No. | Characteristics ^{1 2} | Symbol | Expression ³ | Min. | Max. | Condition | Unit |
|-----|--------------------------------|-------------|----------------------------------|--------------|--------|--------------|------|
| 62 | Clock cycle ⁴ | t_{SSICC} | $4 \times T_C$ $4 \times T_C$ | 30.0 30.0 | — — | i ck i ck | ns |
| 63 | Clock high period | — | — | — | — | — | ns |
| | For internal clock | — | $2 \times T_C - 9.0$ | 6 | — | — | |
| | For external clock | — | $2 \times T_C$ | 15 | — | — | |
| 64 | Clock low period | — | — | — | — | — | ns |
| | For internal clock | — | $2 \times T_C - 9.0$ | 6 | — | — | |
| | For external clock | — | $2 \times T_C$ | 15 | — | — | |

Table 55. ESAI General Timing Requirements (continued)

| No. | Characteristics ^{1 2} | Symbol | Expression ³ | Min. | Max. | Condition | Unit |
|-----|---|--------|-------------------------|--------------|--------------|----------------|------|
| 65 | SCKR rising edge to FSR out (bl) high | — | — | — | 17.0 7.0 | x ck i ck a | ns |
| 66 | SCKR rising edge to FSR out (bl) low | — | — | — | 17.0 7.0 | x ck i ck a | ns |
| 67 | SCKR rising edge to FSR out (wr) high ⁵ | — | — | — | 19.0 9.0 | x ck i ck a | ns |
| 68 | SCKR rising edge to FSR out (wr) low ⁵ | — | — | — | 19.0 9.0 | x ck i ck a | ns |
| 69 | SCKR rising edge to FSR out (wl) high | — | — | — | 16.0 6.0 | x ck i ck a | ns |
| 70 | SCKR rising edge to FSR out (wl) low | — | — | — | 17.0 7.0 | x ck i ck a | ns |
| 71 | Data in setup time before SCKR (SCK in synchronous mode) falling edge | — | — | 12.0 19.0 | — | x ck i ck | ns |
| 72 | Data in hold time after SCKR falling edge | — | — | 3.5 9.0 | — | x ck i ck | ns |
| 73 | FSR input (bl, wr) high before SCKR falling edge ⁵ | — | — | 2.0 12.0 | — | x ck i ck a | ns |
| 74 | FSR input (wl) high before SCKR falling edge | — | — | 2.0 12.0 | — | x ck i ck a | ns |
| 75 | FSR input hold time after SCKR falling edge | — | — | 2.5 8.5 | — | x ck i ck a | ns |
| 76 | Flags input setup before SCKR falling edge | — | — | 0.0 19.0 | — | x ck i ck s | ns |
| 77 | Flags input hold time after SCKR falling edge | — | — | 6.0 0.0 | — | x ck i ck s | ns |
| 78 | SCKT rising edge to FST out (bl) high | — | — | — | 18.0 8.0 | x ck i ck | ns |
| 79 | SCKT rising edge to FST out (bl) low | — | — | — | 20.0 10.0 | x ck i ck | ns |
| 80 | SCKT rising edge to FST out (wr) high ⁵ | — | — | — | 20.0 10.0 | x ck i ck | ns |
| 81 | SCKT rising edge to FST out (wr) low ⁵ | — | — | — | 22.0 12.0 | x ck i ck | ns |
| 82 | SCKT rising edge to FST out (wl) high | — | — | — | 19.0 9.0 | x ck i ck | ns |
| 83 | SCKT rising edge to FST out (wl) low | — | — | — | 20.0 10.0 | x ck i ck | ns |
| 84 | SCKT rising edge to data out enable from high impedance | — | — | — | 22.0 17.0 | x ck i ck | ns |
| 85 | SCKT rising edge to transmitter #0 drive enable assertion | — | — | — | 17.0 11.0 | x ck i ck | ns |

Table 55. ESAI General Timing Requirements (continued)

| No. | Characteristics ^{1 2} | Symbol | Expression ³ | Min. | Max. | Condition | Unit |
|-----|---|--------|-------------------------|-------------|--------------|--------------|------|
| 86 | SCKT rising edge to data out valid | — | — | — | 18.0 13.0 | x ck i ck | ns |
| 87 | SCKT rising edge to data out high impedance ⁶ | — | — | — | 21.0 16.0 | x ck i ck | ns |
| 88 | SCKT rising edge to transmitter #0 drive enable negation ⁶ | — | — | — | 14.0 9.0 | x ck i ck | ns |
| 89 | FST input (bl, wr) setup time before SCKT falling edge ⁵ | — | — | 2.0 18.0 | — — | x ck i ck | ns |
| 90 | FST input (wl) setup time before SCKT falling edge | — | — | 2.0 18.0 | — — | x ck i ck | ns |
| 91 | FST input hold time after SCKT falling edge | — | — | 4.0 5.0 | — — | x ck i ck | ns |
| 92 | FST input (wl) to data out enable from high impedance | — | — | — | 21.0 | — | ns |
| 93 | FST input (wl) to transmitter #0 drive enable assertion | — | — | — | 14.0 | — | ns |
| 94 | Flag output valid after SCKT rising edge | — | — | — — | 14.0 9.0 | x ck i ck | ns |
| 95 | HCKR/HCKT clock cycle | — | $2 \times T_C$ | 15 | — | — | ns |
| 96 | HCKT input rising edge to SCKT output | — | — | — | 18.0 | — | ns |
| 97 | HCKR input rising edge to SCKR output | — | — | — | 18.0 | — | ns |

¹ $V_{CORE_VDD} = 1.00 \pm 0.10$ V; $T_J = -40$ °C to 125 °C, $C_L = 50$ pF

² In the “Characteristics” column, bl = bit length, wl = word length, wr = word length relative

³ In the “Expression” column, $T_C = 7.5$ ns.

⁴ For the internal clock, the external clock cycle is defined by l_{cy}c and the ESAI control register.

⁵ The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but spreads starting from one serial clock before the first bit clock (same as the bit length frame sync signal), until the second-to-last bit-clock of the first word in the frame.

⁶ Periodically sampled and not 100% tested.

3.6.8 Enhanced Secured Digital Host Controller (eSDHCv2) Timing

Figure 54 shows eSDHCv2 timing, and Table 56 describes the timing parameters (SD1–SD8) used in the figure. The following definitions apply to values and signals described in Table 56:

- LS: low-speed mode. Low-speed card can tolerate clocks up to 400 kHz
- FS: full-speed mode. Full-speed MMC card’s clock can reach 20 MHz; full speed SD/SDIO card clock can reach 25 MHz
- HS: high-speed mode. High-speed MMC card’s clock can reach 52 MHz; SD/SDIO card clock can reach 50 MHz

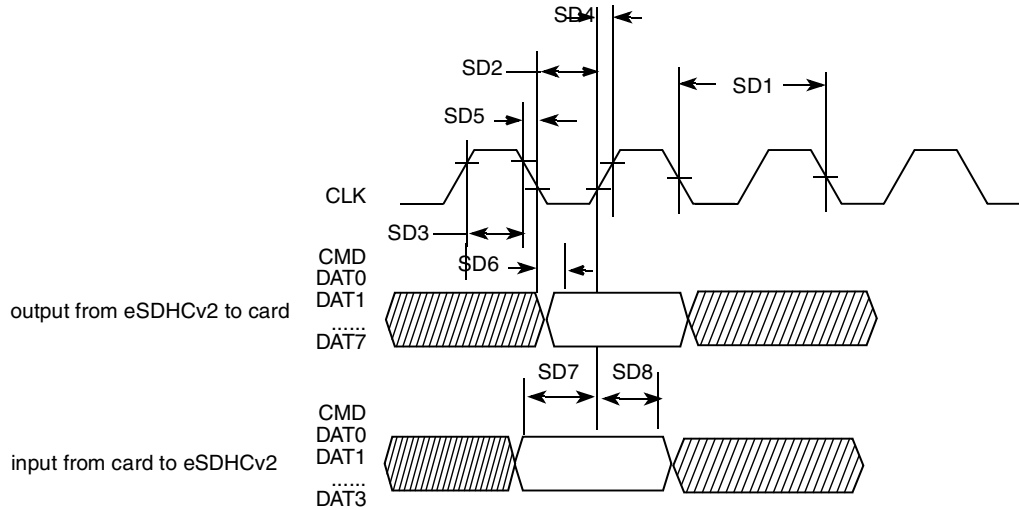


Figure 54. eSDHCv2 Timing

Table 56. eSDHCv2 Interface Timing Specification

| ID | Parameter | Symbols | Min. | Max. | Unit |
|---|---|------------|------|-------|------|
| Card Input Clock | | | | | |
| SD1 | Clock frequency (low speed) | f_{PP}^1 | 0 | 400 | kHz |
| | Clock frequency (SD/SDIO full speed/high speed) | f_{PP}^2 | 0 | 25/50 | MHz |
| | Clock frequency (MMC full speed/high speed) | f_{PP}^3 | 0 | 20/52 | MHz |
| | Clock frequency (identification mode) | f_{OD} | 100 | 400 | kHz |
| SD2 | Clock low time | t_{WL} | 7 | — | ns |
| SD3 | Clock high time | t_{WH} | 7 | — | ns |
| SD4 | Clock rise time | t_{TLH} | — | 3 | ns |
| SD5 | Clock fall time | t_{THL} | — | 3 | ns |
| eSDHC Output / Card Inputs CMD, DAT (Reference to CLK) | | | | | |
| SD6 | eSDHC output delay | t_{OD} | -3 | 3 | ns |
| eSDHC Input / Card Outputs CMD, DAT (Reference to CLK) | | | | | |
| SD7 | eSDHC input setup time | t_{ISU} | 2.5 | — | ns |
| SD8 | eSDHC input hold time | t_{IH}^4 | 2.5 | — | ns |

¹ In low-speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

² In normal-speed mode for SD/SDIO card, clock frequency can be any value between 0 ~ 25 MHz. In high speed mode, clock frequency can be any value between 0 ~ 50 MHz.

³ In normal-speed mode for MMC card, clock frequency can be any value between 0 ~ 20 MHz. In high speed mode, clock frequency can be any value between 0 ~ 52 MHz.

⁴ To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

3.6.9 Fast Ethernet Controller (FEC) Timing

The FEC is designed to support both 10- and 100-Mbps Ethernet networks compliant with the IEEE 802.3 standard. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports 10/100 Mbps MII (18 pins altogether), 10/100 Mbps RMII (ten pins, including serial management interface) and the 10 Mbps-only 7-Wire interface (which uses seven of the MII pins), for connection to an external Ethernet transceiver. All signals are compatible with transceivers operating at a voltage of 3.3 V.

The following subsections describe the timing for MII and RMII modes.

3.6.9.1 FEC MII Mode Timing

The following subsections describe MII receive, transmit, asynchronous inputs, and serial management signal timings.

3.6.9.1.1 MII Receive Signal Timing (FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER, and FEC_RX_CLK)

The receiver functions correctly up to an FEC_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the FEC_RX_CLK frequency.

Figure 55 shows MII receive signal timings. Table 57 describes the timing parameters (M1–M4) shown in the figure.

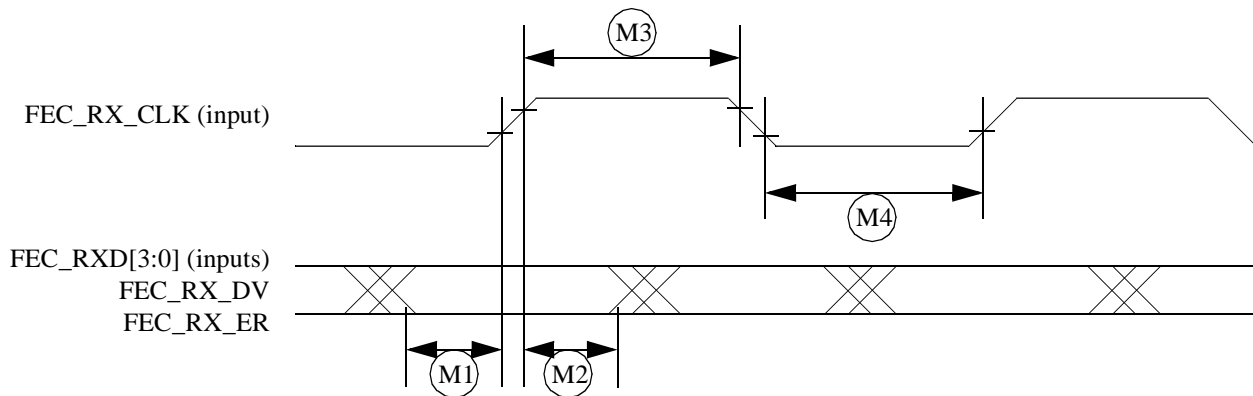


Figure 55. MII Receive Signal Timing Diagram

Table 57. MII Receive Signal Timing

| ID | Characteristic ¹ | Min. | Max. | Unit |
|----|--|------|------|-------------------|
| M1 | FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER to FEC_RX_CLK setup | 5 | — | ns |
| M2 | FEC_RX_CLK to FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER hold | 5 | — | ns |
| M3 | FEC_RX_CLK pulse width high | 35% | 65% | FEC_RX_CLK period |
| M4 | FEC_RX_CLK pulse width low | 35% | 65% | FEC_RX_CLK period |

¹ FEC_RX_DV, FEC_RX_CLK, and FEC_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

3.6.9.1.2 MII Transmit Signal Timing (FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER, and FEC_TX_CLK)

The transmitter functions correctly up to an FEC_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the FEC_TX_CLK frequency.

Figure 56 shows MII transmit signal timings. Table 58 describes the timing parameters (M5–M8) shown in the figure.

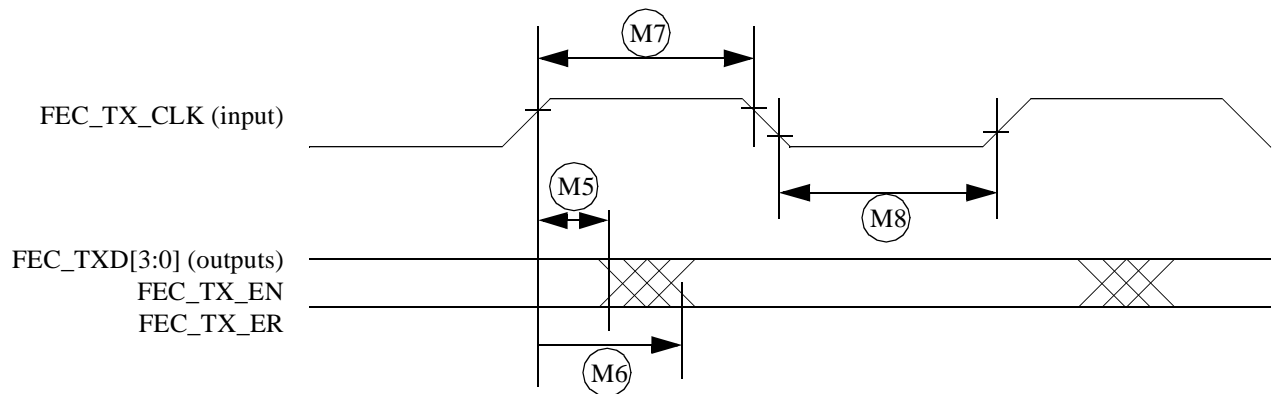


Figure 56. MII Transmit Signal Timing Diagram

Table 58. MII Transmit Signal Timing

| ID | Characteristic ¹ | Min. | Max. | Unit |
|----|--|------|------|-------------------|
| M5 | FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER invalid | 5 | — | ns |
| M6 | FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER valid | — | 20 | ns |
| M7 | FEC_TX_CLK pulse width high | 35% | 65% | FEC_TX_CLK period |
| M8 | FEC_TX_CLK pulse width low | 35% | 65% | FEC_TX_CLK period |

¹ FEC_TX_EN, FEC_TX_CLK, and FEC_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

3.6.9.1.3 MII Asynchronous Inputs Signal Timing (FEC_CRIS and FEC_COL)

Figure 57 shows MII asynchronous input timings. Table 59 describes the timing parameter (M9) shown in the figure.

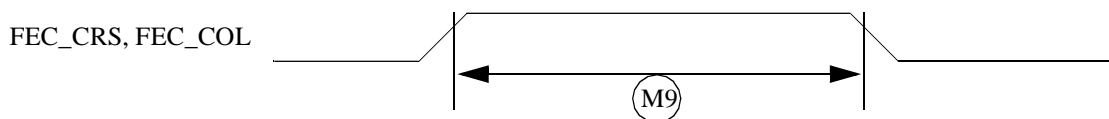


Figure 57. MII Async Inputs Timing Diagram

Table 59. MII Asynchronous Inputs Signal Timing

| ID | Characteristic | Min. | Max. | Unit |
|-----------------|--|------|------|-------------------|
| M9 ¹ | FEC_CRG to FEC_COL minimum pulse width | 1.5 | — | FEC_TX_CLK period |

¹ FEC_COL has the same timing in 10-Mbit 7-wire interface mode.

3.6.9.2 MII Serial Management Channel Timing (FEC_MDIO and FEC_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to comply with the IEEE 802.3 standard MII specification. However the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Figure 58 shows MII asynchronous input timings. Table 60 describes the timing parameters (M10—M15) shown in the figure.

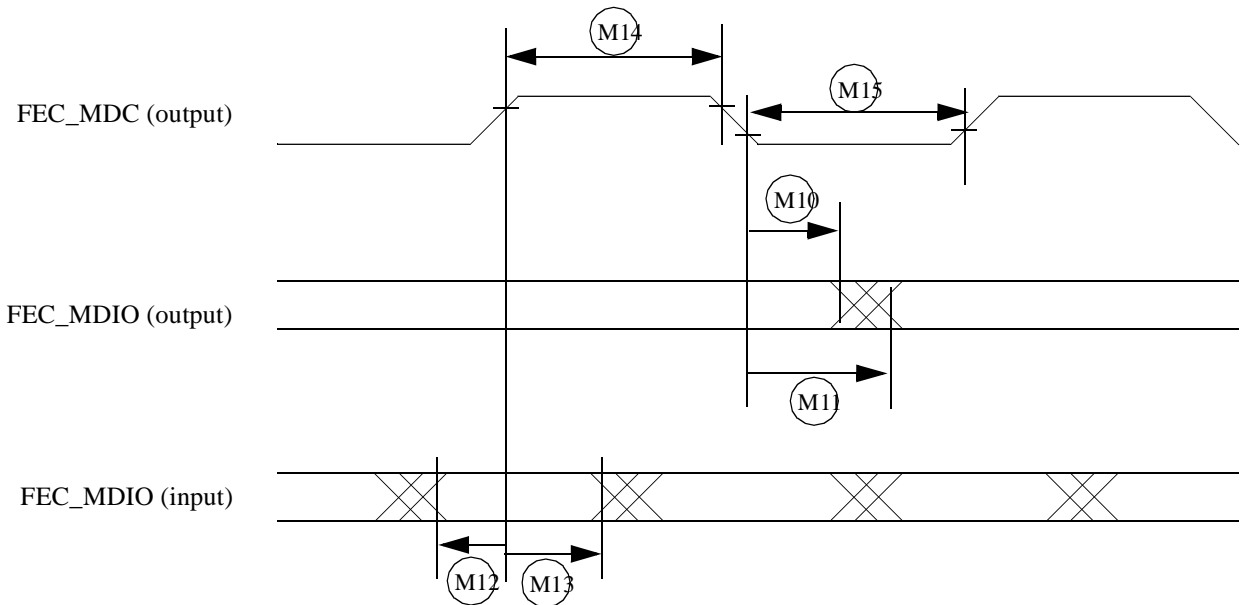


Figure 58. MII Serial Management Channel Timing Diagram

Table 60. MII Serial Management Channel Timing

| ID | Characteristic | Min. | Max. | Unit |
|-----|--|------|------|----------------|
| M10 | FEC_MDC falling edge to FEC_MDIO output invalid (min. propagation delay) | 0 | — | ns |
| M11 | FEC_MDC falling edge to FEC_MDIO output valid (max. propagation delay) | — | 5 | ns |
| M12 | FEC_MDIO (input) to FEC_MDC rising edge setup | 18 | — | ns |
| M13 | FEC_MDIO (input) to FEC_MDC rising edge hold | 0 | — | ns |
| M14 | FEC_MDC pulse width high | 40% | 60% | FEC_MDC period |
| M15 | FEC_MDC pulse width low | 40% | 60% | FEC_MDC period |

3.6.9.3 RMII Mode Timing

In RMII mode, FEC_TX_CLK is used as the REF_CLK, which is a 50 MHz \pm 50 ppm continuous reference clock. FEC_RX_DV is used as the CRS_DV in RMII. Other signals under RMII mode include FEC_TX_EN, FEC_TXD[1:0], FEC_RXD[1:0] and FEC_RX_ER.

Figure 59 shows RMII mode timings. Table 61 describes the timing parameters (M16–M21) shown in the figure.

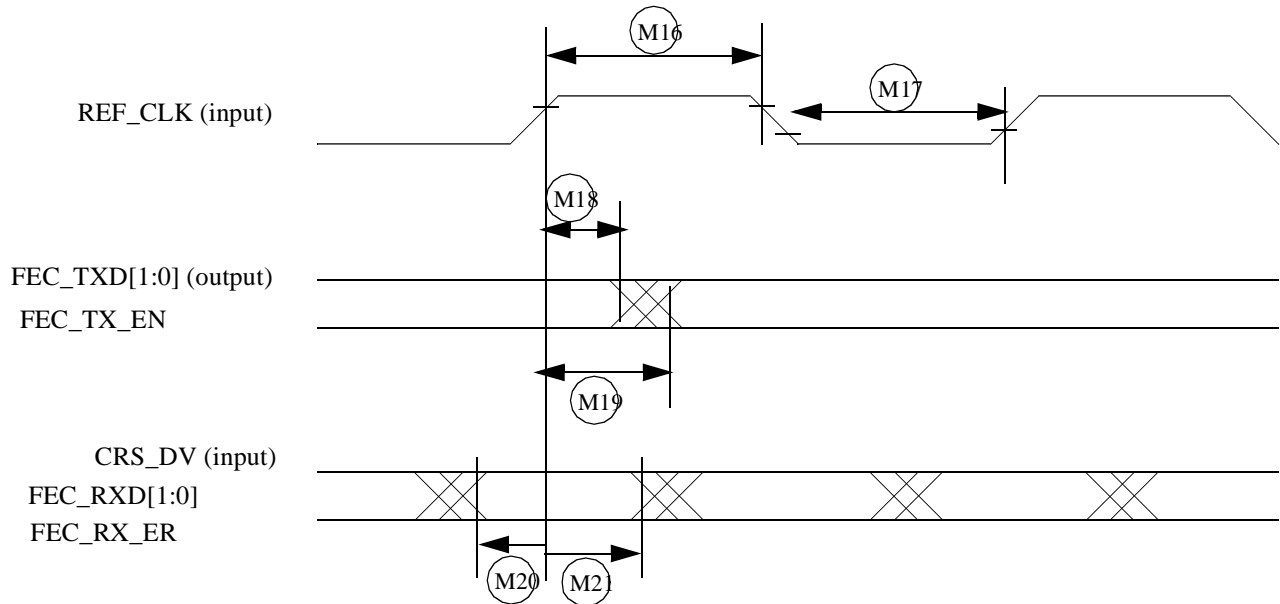


Figure 59. RMII Mode Signal Timing Diagram

Table 61. RMII Signal Timing

| ID | Characteristic | Min. | Max. | Unit |
|-----|---|------|------|----------------|
| M16 | REF_CLK(FEC_TX_CLK) pulse width high | 35% | 65% | REF_CLK period |
| M17 | REF_CLK(FEC_TX_CLK) pulse width low | 35% | 65% | REF_CLK period |
| M18 | REF_CLK to FEC_TXD[1:0], FEC_TX_EN invalid | 3 | — | ns |
| M19 | REF_CLK to FEC_TXD[1:0], FEC_TX_EN valid | — | 12 | ns |
| M20 | FEC_RXD[1:0], CRS_DV(FEC_RX_DV), FEC_RX_ER to REF_CLK setup | 2 | — | ns |
| M21 | REF_CLK to FEC_RXD[1:0], FEC_RX_DV, FEC_RX_ER hold | 2 | — | ns |

3.6.10 Controller Area Network (FlexCAN) Transceiver Parameters and Timing

Table 62 and Table 63 show voltage requirements for the FlexCAN transceiver Tx and Rx pins.

Table 62. Tx Pin Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---------------------------|--------|------|------|------------------|-------|
| High-level output voltage | VOH | 2 | — | $V_{CC}^1 + 0.3$ | V |
| Low-level output voltage | VOL | — | 0.8 | — | V |

¹ $V_{CC} = +3.3\text{ V} \pm 5\%$

Table 63. Rx Pin Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|--------------------------|--------|-----------------------|------|------------|-------|
| High-level input voltage | VIH | $0.8 \times V_{CC}^1$ | — | V_{CC}^1 | V |
| Low-level input voltage | VIL | — | 0.4 | — | V |

¹ $V_{CC} = +3.3\text{ V} \pm 5\%$

Figure 60 through Figure 63 show the FlexCAN timing, including timing of the standby and shutdown signals.

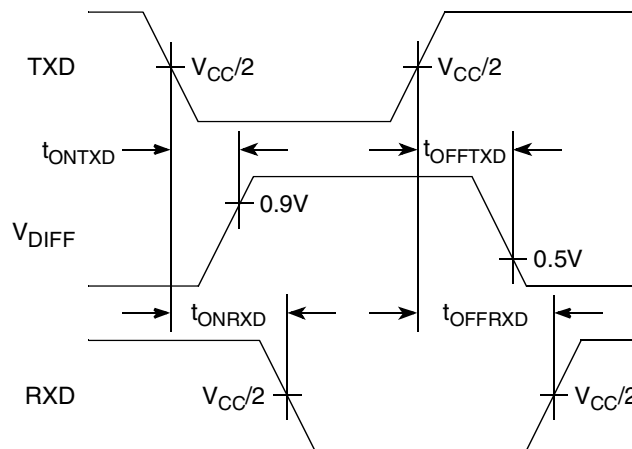


Figure 60. FlexCAN Timing Diagram

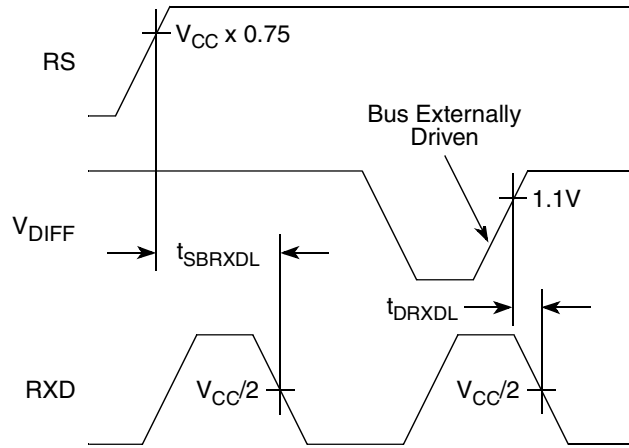


Figure 61. Timing Diagram for FlexCAN Standby Signal

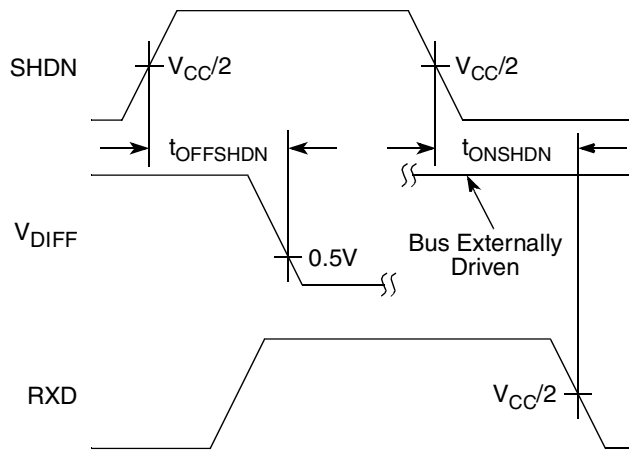


Figure 62. Timing Diagram for FlexCAN Shutdown Signal

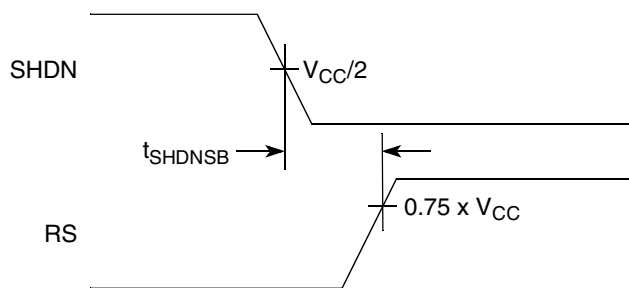


Figure 63. Timing Diagram for FlexCAN Shutdown-to-Standby Signal

Because integer multiples are not possible taking into account the range of frequencies the SoC has to operate, DPLLs will work in FOL mode only.

3.6.11 Inter IC Communication (I²C) Timing

The I²C communication protocol consists of the following seven elements:

- Start
- Data source/recipient
- Data direction
- Slave acknowledge
- Data
- Data acknowledge
- Stop

Figure 64 shows the timing of the I²C module. Table 64 and Table 65 describe the I²C module timing parameters (IC1–IC6) shown in the figure.

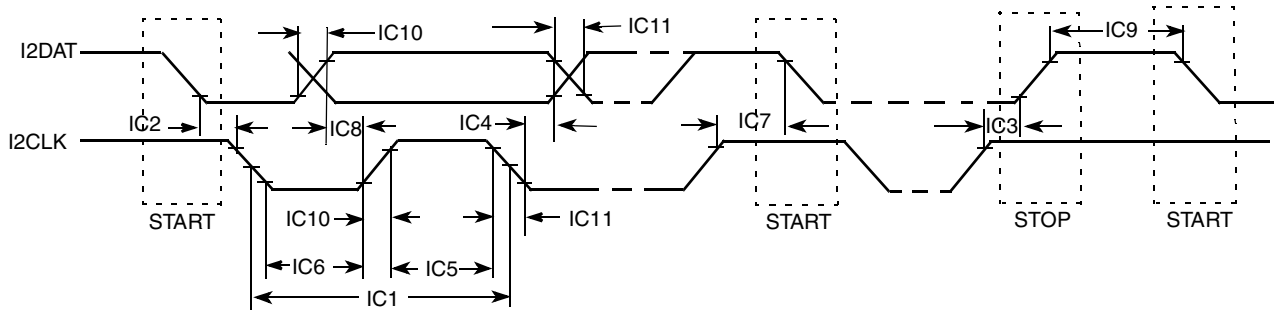


Figure 64. I²C Module Timing Diagram

Table 64. I2C Module Timing Parameters: 3.0 V +/-0.30 V

| ID | Parameter | Standard Mode | | Fast Mode | | Unit |
|------|---|----------------|-------------------|-----------------------------------|------------------|------|
| | | Min. | Max. | Min. | Max. | |
| IC1 | I2CLK cycle time | 10 | - | 2.5 | - | μs |
| IC2 | Hold time (repeated) START condition | 4.0 | - | 0.6 | - | μs |
| IC3 | Set-up time for STOP condition | 4.0 | - | 0.6 | - | μs |
| IC4 | Data hold time | 0 ¹ | 3.45 ² | 0 ¹ | 0.9 ² | μs |
| IC5 | HIGH Period of I2CLK Clock | 4.0 | - | 0.6 | - | μs |
| IC6 | LOW Period of the I2CLK Clock | 4.7 | - | 1.3 | - | μs |
| IC7 | Set-up time for a repeated START condition | 4.7 | - | 0.6 | - | μs |
| IC8 | Data set-up time | 250 | - | 100 ³ | - | ns |
| IC9 | Bus free time between a STOP and START condition | 4.7 | - | 1.3 | - | μs |
| IC10 | Rise time of both I2DAT and I2CLK signals | - | 1000 | 20+0.1C _b ⁴ | 300 | ns |
| IC11 | Fall time of both I2DAT and I2CLK signals | - | 300 | 20+0.1C _b ⁴ | 300 | ns |
| IC12 | Capacitive load for each bus line (C _b) | - | 400 | - | 400 | pF |

¹ A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

- ² The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal
- ³ A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line $\text{max_rise_time}(\text{ID No IC9}) + \text{data_setup_time}(\text{ID No IC7}) = 1000 + 250 = 1250 \text{ ns}$ (according to the Standard-mode I2C-bus specification) before the I2CLK line is released.
- ⁴ C_b = total capacitance of one bus line in pF.

Table 65. I2C Module Timing Parameters: 1.8 V +/- 0.10 V

| ID | Parameter | Standard Mode | | Unit |
|------|--|----------------|-------------------|------|
| | | Min. | Max. | |
| IC1 | I2CLK cycle time | 10 | - | μs |
| IC2 | Hold time (repeated) START condition | 4.0 | - | μs |
| IC3 | Set-up time for STOP condition | 4.0 | - | μs |
| IC4 | Data hold time | 0 ¹ | 3.45 ² | μs |
| IC5 | HIGH Period of I2CLK Clock | 4.0 | - | μs |
| IC6 | LOW Period of the I2CLK Clock | 4.7 | - | μs |
| IC7 | Set-up time for a repeated START condition | 4.7 | - | μs |
| IC8 | Data set-up time | 250 | - | ns |
| IC9 | Bus free time between a STOP and START condition | 4.7 | - | μs |
| IC10 | Rise time of both I2DAT and I2CLK signals | - | 1000 | ns |
| IC11 | Fall time of both I2DAT and I2CLK signals | - | 300 | ns |
| IC12 | Capacitive load for each bus line (C_b) | - | 400 | pF |

- ¹ A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.
- ² The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal

3.6.12 Liquid Crystal Display Controller (LCDC) Timing

Figure 65 and Figure 66 show LCDC timing in non-TFT and TFT mode respectively, and Table 66 and Table 67 list the timing parameters used in the associated figures.

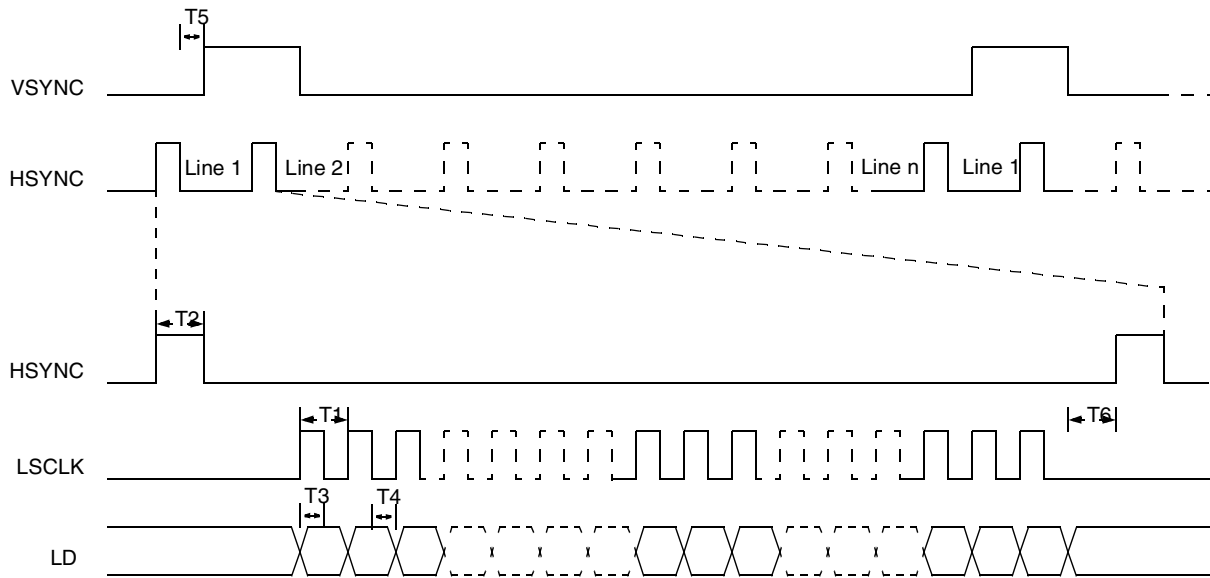


Figure 65. LCDC Non-TFT Mode Timing Diagram

Table 66. LCDC Non-TFT Mode Timing Parameters

| ID | Description | Min. | Max. | Unit |
|----|--|------|------|-------|
| T1 | Pixel clock period | 22.5 | 1000 | ns |
| T2 | HSYNC width | 1 | — | T^1 |
| T3 | LD setup time | 5 | — | ns |
| T4 | LD hold time | 5 | — | ns |
| T5 | Wait between HSYNC and VSYNC rising edge | 2 | — | T^1 |
| T6 | Wait between last data and HSYNC rising edge | 1 | — | T^1 |

¹ T is pixel clock period

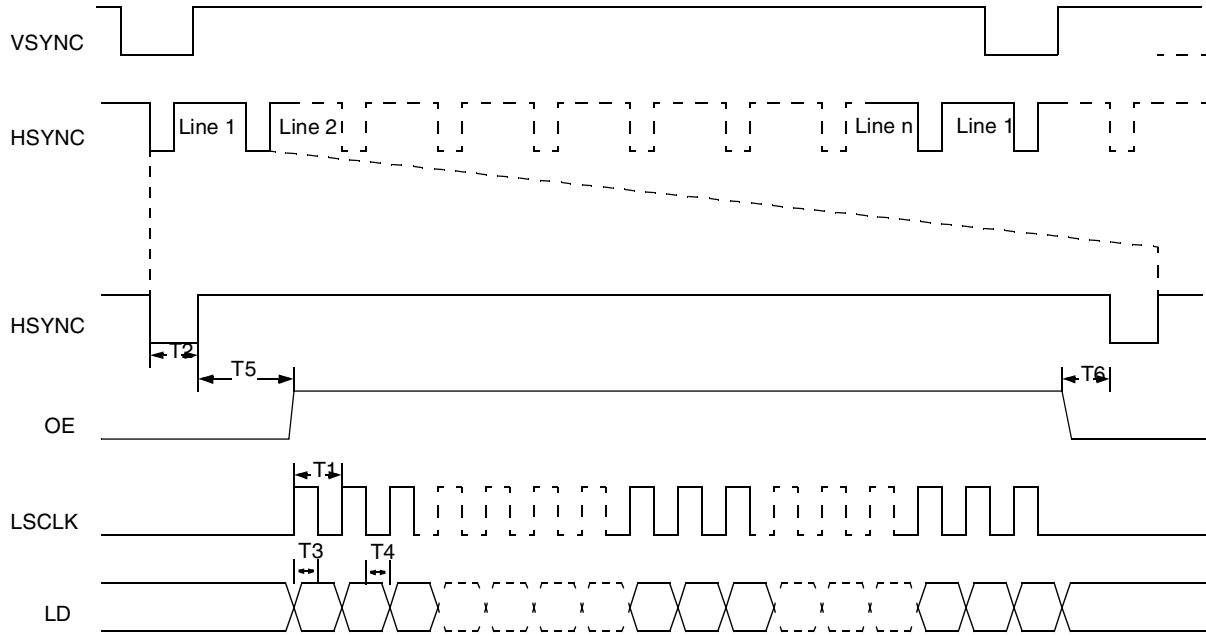


Figure 66. LCDC TFT Mode Timing Diagram

Table 67. LCDC TFT Mode Timing Parameters

| ID | Description | Min. | Ma | Unit |
|----|--|------|------|----------------|
| T1 | Pixel clock period | 22.5 | 1000 | ns |
| T2 | HSYNC width | 1 | — | T ¹ |
| T3 | LD setup time | 5 | — | ns |
| T4 | LD hold time | 5 | — | ns |
| T5 | Delay from the end of HSYNC to the beginning of the OE pulse | 3 | — | T ¹ |
| T6 | Delay from end of OE to the beginning of the HSYNC pulse | 1 | — | T ¹ |

¹ T is pixel clock period

3.6.13 Pulse Width Modulator (PWM) Timing Parameters

Figure 67 depicts the timing of the PWM, and Table 68 lists the PWM timing characteristics.

The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse width modulator output (PWMO) external pin.

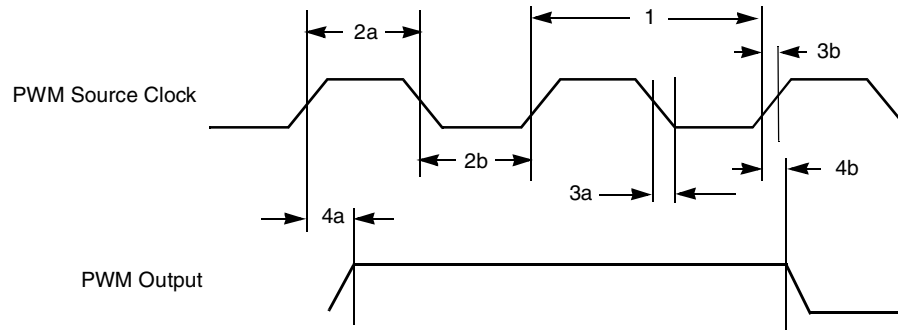


Figure 67. PWM Timing

Table 68. PWM Output Timing Parameter

| Ref No. | Parameter | Minimum | Maximum | Unit |
|---------|-----------------------------------|---------|---------|------|
| 1 | System CLK frequency ¹ | 0 | ipg_clk | MHz |
| 2a | Clock high time | 12.29 | — | ns |
| 2b | Clock low time | 9.91 | — | ns |
| 3a | Clock fall time | — | 0.5 | ns |
| 3b | Clock rise time | — | 0.5 | ns |
| 4a | Output delay time | — | 9.37 | ns |
| 4b | Output setup time | 8.71 | — | ns |

¹ CL of PWMO = 30 pF

3.6.14 Subscriber Identity Module (SIM) Timing

Each SIM module interface consists of a total of 12 pins (two separate ports, each containing six signals). Typically a port uses five signals.

The interface is designed to be used with synchronous SIM cards, meaning the SIM module provides the clock used by the SIM card. The clock frequency is typically 372 times the Tx/Rx data rate; however, the SIM module can also work with CLK frequencies of 16 times the Tx/Rx data rate.

There is no timing relationship between the clock and the data. The clock that the SIM module provides to the SIM card is used by the SIM card to recover the clock from the data in the same manner as standard UART data exchanges. All six signals (five for bidirectional Tx/Rx) of the SIM module are asynchronous with each other.

There are no required timing relationships between signals in normal mode. The SIM card is initiated by the interface device; the SIM card responds with Answer to Reset. Although the SIM interface has no defined requirements, the ISO/IEC 7816 defines reset and power-down sequences (for detailed information see ISO/IEC 7816).

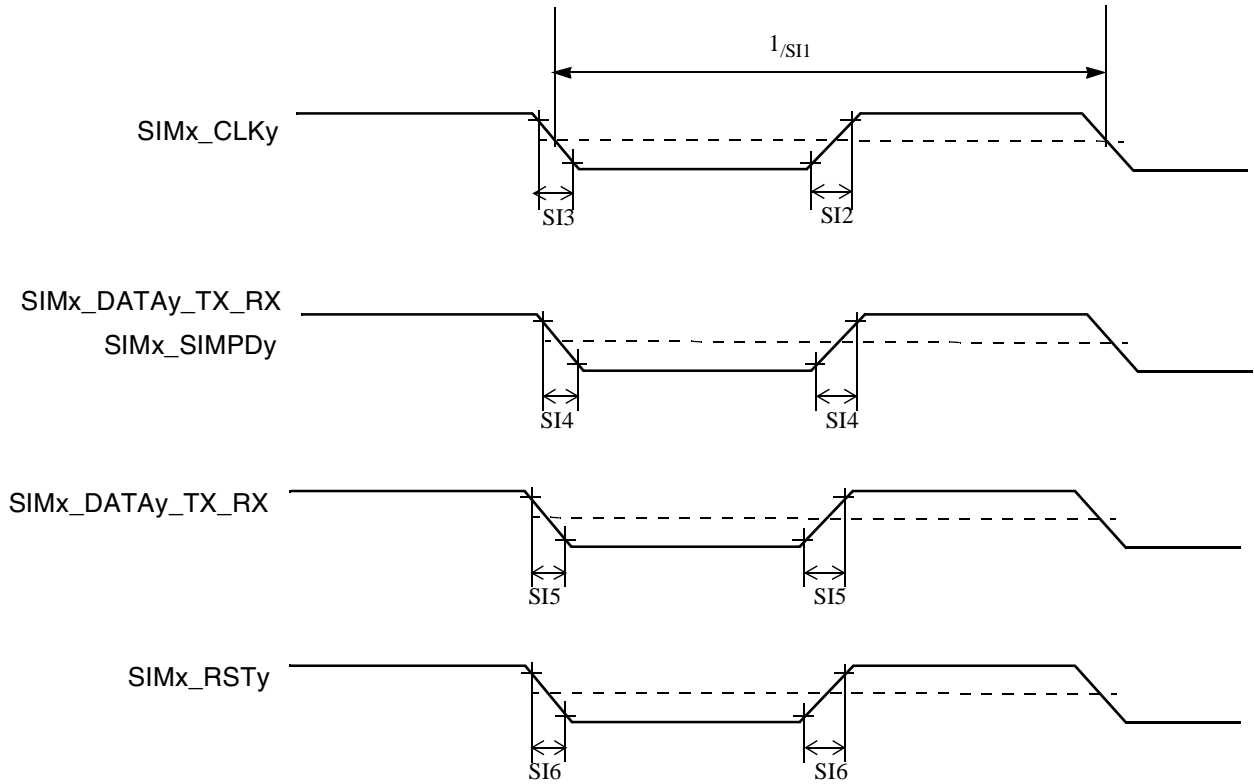


Figure 68. SIM Clock Timing Diagram

Table 69 defines the general timing requirements for the SIM interface.

Table 69. Timing Specifications, High Drive Strength

| ID | Parameter | Symbol | Min. | Max. | Unit |
|-----|---|-------------|------|----------------------------|------|
| SI1 | SIM clock frequency (SIMx_CLKy) ¹ | S_{freq} | 0.01 | 25 | MHz |
| SI2 | SIM clock rise time (SIMx_CLKy) ² | S_{rise} | — | $0.09 \times (1/S_{freq})$ | ns |
| SI3 | SIM clock fall time (SIMx_CLKy) ³ | S_{fall} | — | $0.09 \times (1/S_{freq})$ | ns |
| SI4 | SIM input transition time (SIMx_DATAy_RX_TX, SIMx_SIMPDy) | S_{trans} | 10 | 25 | ns |
| SI5 | SIM I/O rise time / fall time (SIMx_DATAy_RX_TX) ⁴ | Tr/Tf | — | 1 | us |
| SI6 | SIM RST rise time / fall time (SIMx_RSTy) ⁵ | Tr/Tf | — | 1 | us |

¹ 50% duty cycle clock,

² With C = 50 pF

³ With C = 50 pF

⁴ With Cin = 30 pF, Cout = 30 pF,

⁵ With Cin = 30 pF,

3.6.14.1 SIM Reset Sequences

SIM cards may have internal reset, or active low reset. The following subset describes the reset sequences in these two cases.

3.6.14.1.1 SIM Cards with Internal Reset

Figure 69 shows the reset sequence for SIM cards with internal reset. The reset sequence comprises the following steps:

- After power-up, the clock signal is enabled on SIMx_CLKy (time T0)
- After 200 clock cycles, SIMx_DATAy_RX_TX must be asserted.
- The card must send a response on SIMx_DATAy_RX_TX acknowledging the reset between 400–40000 clock cycles after T0.

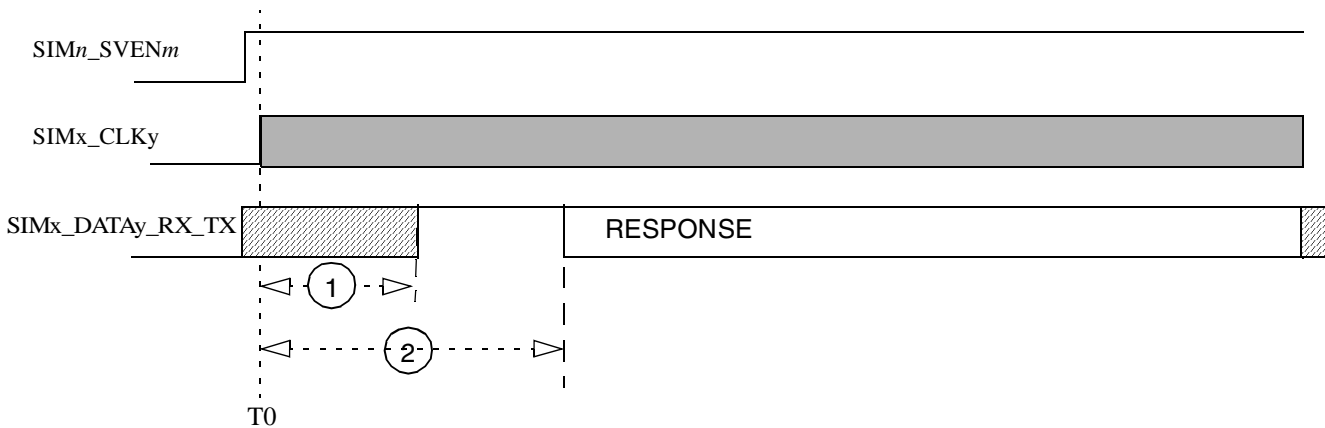


Figure 69. Internal Reset Card Reset Sequence

Table 70 defines the general timing requirements for the SIM interface.

Table 70. Timing Specifications, Internal Reset Card Reset Sequence

| Ref No. | Min. | Max. | Units |
|---------|------|--------|------------|
| 1 | — | 200 | clk cycles |
| 2 | 400 | 40,000 | clk cycles |

3.6.14.1.2 SIM Cards with Active Low Reset

Figure 70 shows the reset sequence for SIM cards with active low reset. The reset sequence comprises the following steps:

- After power-up, the clock signal is enabled on SIMx_CLKy (time T0)
- After 200 clock cycles, SIMx_DATAy_RX_TX must be asserted.
- SIMx_RSTy must remain low for at least 40,000 clock cycles after T0 (no response is to be received on RX during those 40,000 clock cycles)
- SIMx_RSTy is asserted (at time T1)
- SIMx_RSTy must remain asserted for at least 40,000 clock cycles after T1, and a response must be received on SIMx_DATAy_RX_TX between 400 and 40,000 clock cycles after T1.

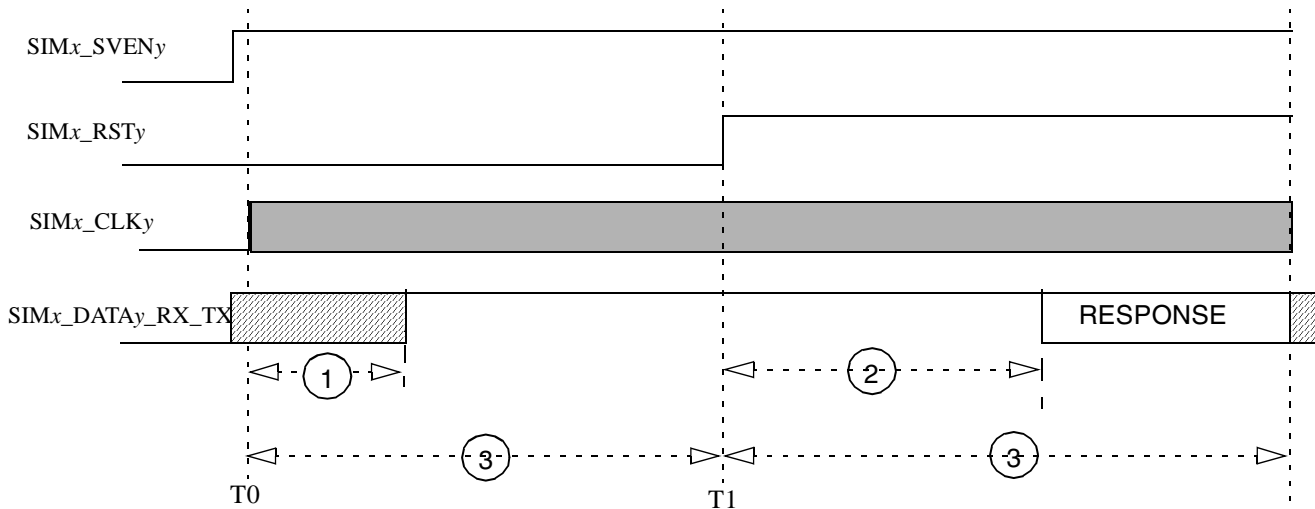


Figure 70. Active-Low-Reset SIM Card Reset Sequence

Table 71 defines the general timing requirements for the SIM interface.

Table 71. Timing Specifications, Active-Low-Reset SIM Card Reset Sequence

| Ref No. | Min. | Max. | Unit |
|---------|--------|--------|------------|
| 1 | — | 200 | clk cycles |
| 2 | 400 | 40,000 | clk cycles |
| 3 | 40,000 | — | clk cycles |

3.6.14.2 SIM Power-Down Sequence

Figure 71 shows the SIM interface power-down AC timing diagram. Table 72 shows the timing requirements for parameters (SI7–SI10) shown in the figure.

The power-down sequence for the SIM interface is as follows:

- SIMx_SIMPDy port detects the removal of the SIM Card
- SIMx_RSTy is negated
- SIMx_CLKy is negated
- SIMx_DATAy_RX_TX is negated
- SIMx_SVENy is negated

Each of the above steps requires one CKIL period (usually 32 kHz). Power-down may be initiated by a SIM card removal detection; or it may be launched by the processor.

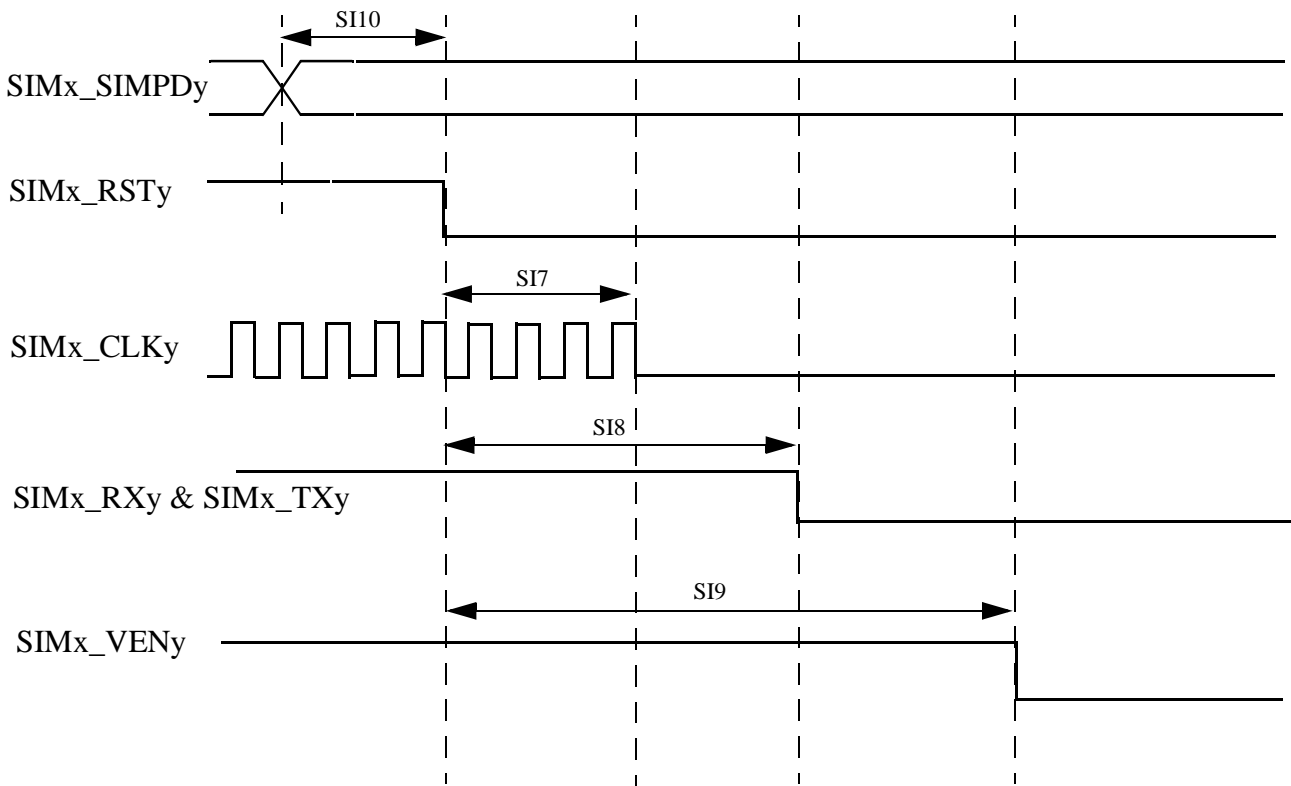


Figure 71. SmartCard Interface Power Down AC Timing

Table 72. Timing Requirements for Power-down Sequence

| ID | PARAMETER | SYMBOL | Min. | Max. | Unit |
|------|--------------------------------------|---------------|-------------------------|-------------------------|------|
| SI7 | SIM reset to SIM clock stop | $S_{rst2clk}$ | $0.9 \times 1/F_{ckil}$ | $1.1 \times 1/F_{ckil}$ | ns |
| SI8 | SIM reset to SIM Tx data low | $S_{rst2dat}$ | $1.8 \times 1/F_{ckil}$ | $2.2 \times 1/F_{ckil}$ | ns |
| SI9 | SIM reset to SIM voltage enable low | $S_{rst2ven}$ | $2.7 \times 1/F_{ckil}$ | $3.3 \times 1/F_{ckil}$ | ns |
| SI10 | SIM presence detect to SIM reset low | S_{pd2rst} | $0.9 \times 1/F_{ckil}$ | $1.1 \times 1/F_{ckil}$ | ns |

3.6.15 System JTAG Controller (SJC) Timing

Figure 72 through Figure 75 show respectively the test clock input, boundary scan, test access port, and TRST timings for the SJC. Table 73 describes the SJC timing parameters (SJ1–SJ13) indicated in the figures.

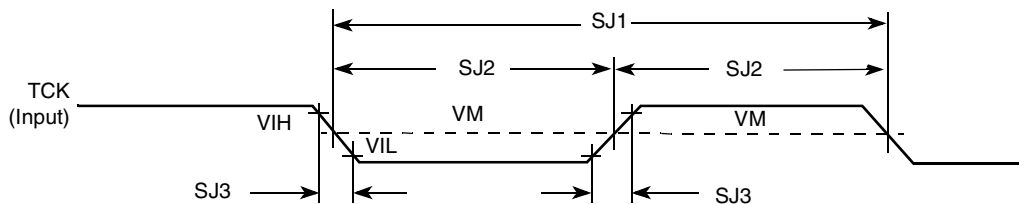


Figure 72. Test Clock Input Timing Diagram

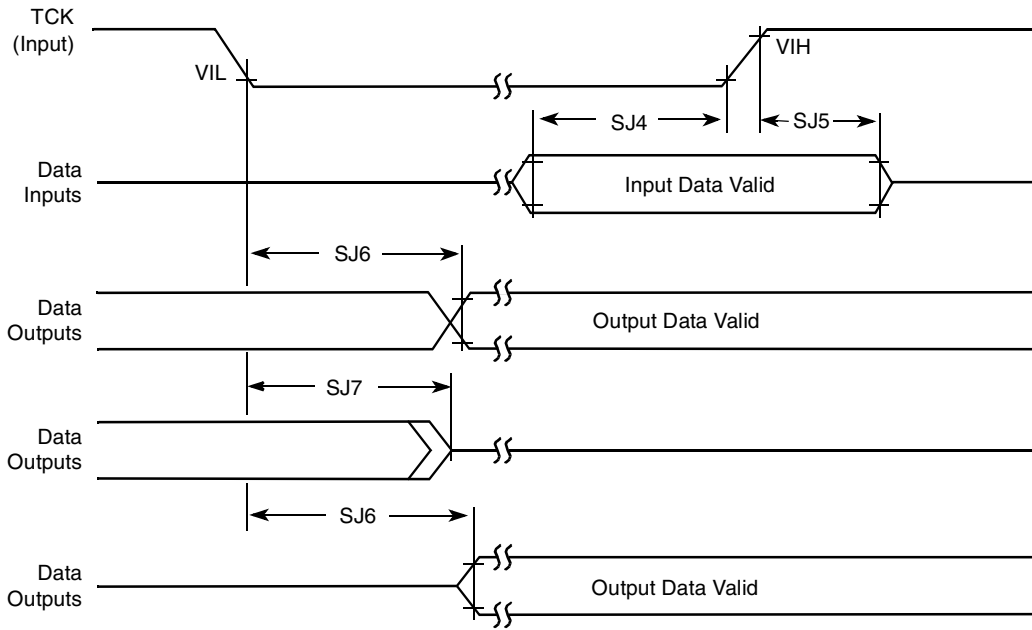


Figure 73. Boundary Scan (JTAG) Timing Diagram

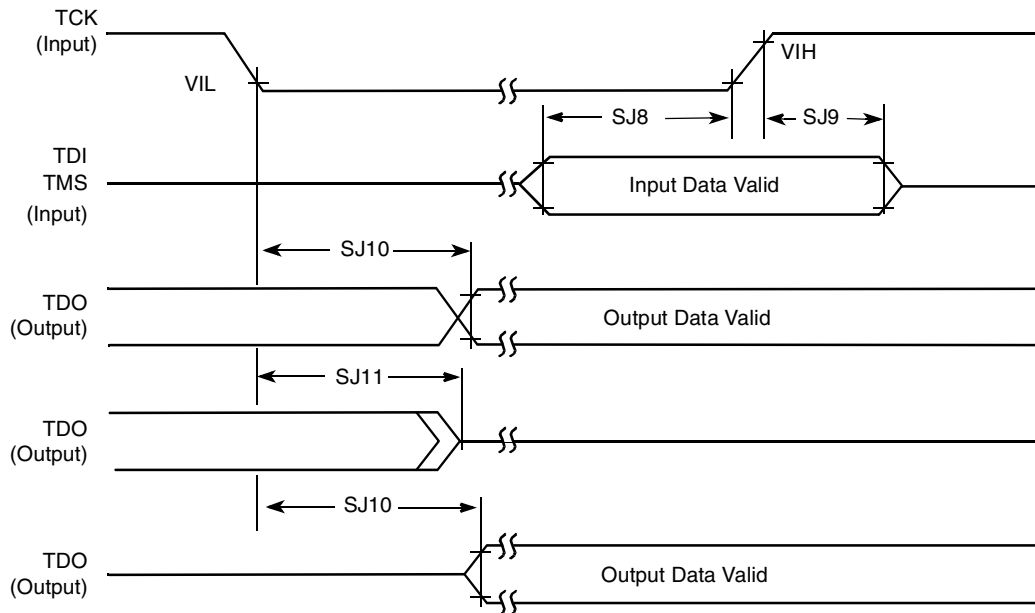


Figure 74. Test Access Port Timing Diagram

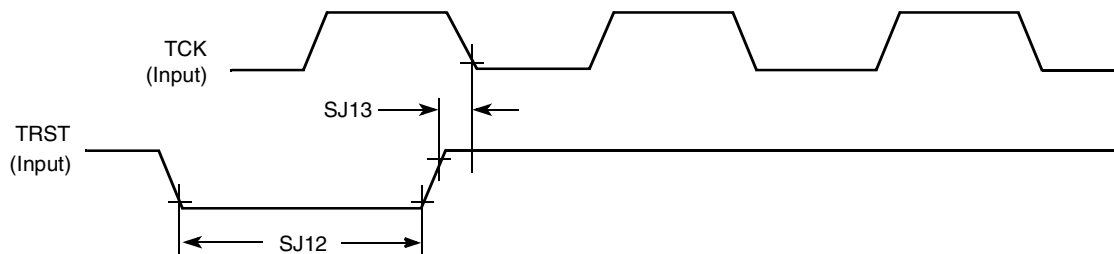


Figure 75. $\overline{\text{TRST}}$ Timing Diagram

Table 73. SJC Timing Parameters

| ID | Parameter | All Frequencies | | Unit |
|------|--|------------------|------|------|
| | | Min. | Max. | |
| SJ1 | TCK cycle time | 100 ¹ | — | ns |
| SJ2 | TCK clock pulse width measured at V_M ² | 40 | — | ns |
| SJ3 | TCK rise and fall times | — | 3 | ns |
| SJ4 | Boundary scan input data set-up time | 10 | — | ns |
| SJ5 | Boundary scan input data hold time | 50 | — | ns |
| SJ6 | TCK low to output data valid | — | 50 | ns |
| SJ7 | TCK low to output high impedance | — | 50 | ns |
| SJ8 | TMS, TDI data set-up time | 10 | — | ns |
| SJ9 | TMS, TDI data hold time | 50 | — | ns |
| SJ10 | TCK low to TDO data valid | — | 44 | ns |
| SJ11 | TCK low to TDO high impedance | — | 44 | ns |
| SJ12 | $\overline{\text{TRST}}$ assert time | 100 | — | ns |
| SJ13 | $\overline{\text{TRST}}$ set-up time to TCK low | 40 | — | ns |

¹ In cases where SDMA TAP is put in the chain, the maximum TCK frequency is limited by the maximum ratio of 1:8 of SDMA core frequency to TCK. This implies a maximum frequency of 8.25 MHz (or 121.2 ns) for a 66 MHz IPG clock.

² V_M - mid point voltage

3.6.16 Smart Liquid Crystal Display Controller (SLCDC)

Figure 76 and Figure 77 show SLCDC timing for serial and parallel transfers respectively. Table 74 and Table 75 describe the timing parameters shown in the respective figures.

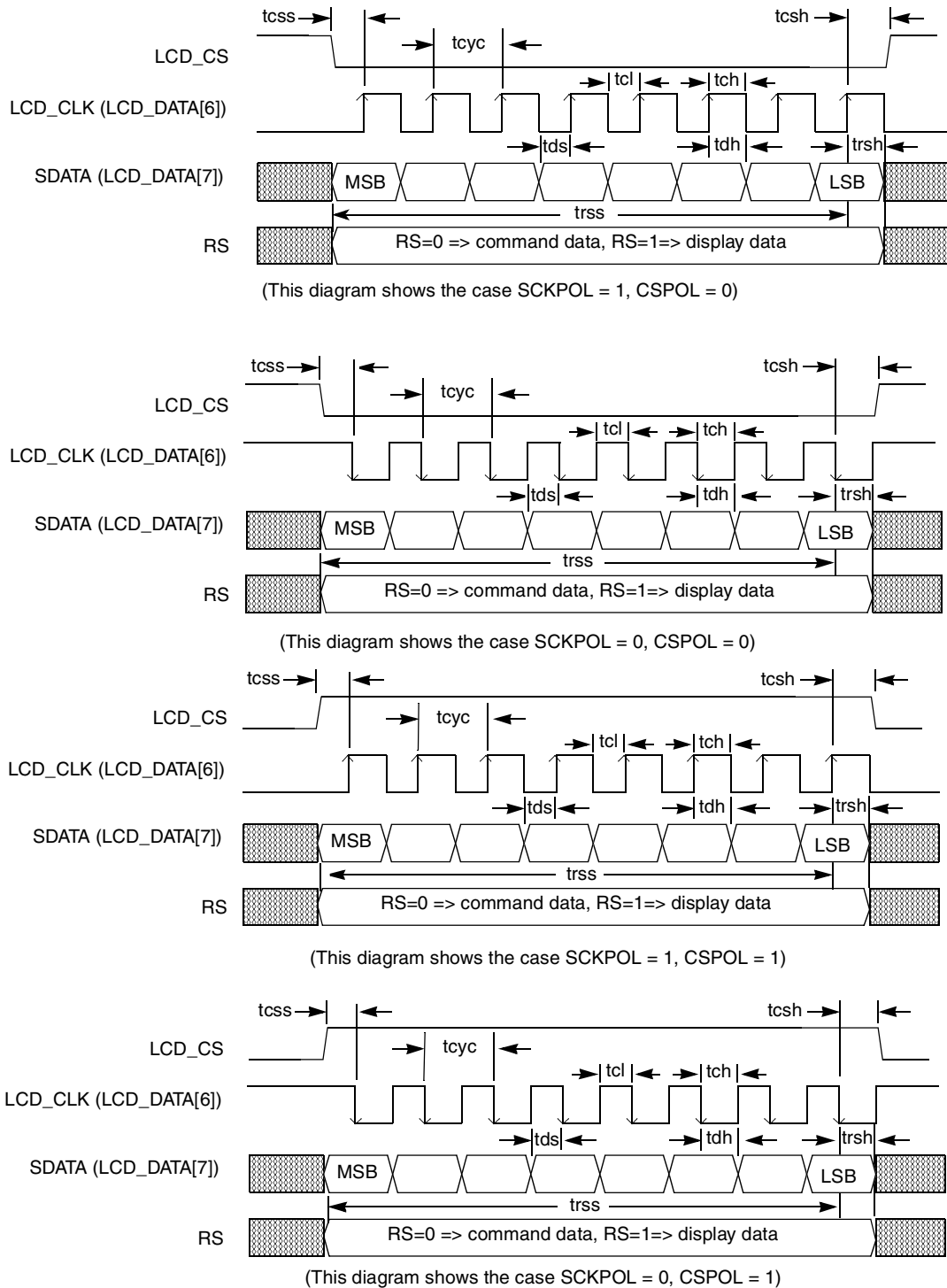


Figure 76. SLCDC Timing Diagram—Serial Transfers to LCD Device

Table 74. SLCDC Serial Interface Timing Parameters

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|-----------|----------------------------|--|------|------|-------|
| t_{css} | Chip select setup time | $(t_{cyc} / 2) (\pm) t_{prop}$ | — | — | ns |
| t_{csh} | Chip select hold time | $(t_{cyc} / 2) (\pm) t_{prop}$ | — | — | ns |
| t_{cyc} | Serial clock cycle time | $39 (\pm) t_{prop}$ | — | 2641 | ns |
| t_{cl} | Serial clock low pulse | $18 (\pm) t_{prop}$ | — | — | ns |
| t_{ch} | Serial clock high pulse | $18 (\pm) t_{prop}$ | — | — | ns |
| t_{ds} | Data setup time | $(t_{cyc} / 2) (\pm) t_{prop}$ | — | — | ns |
| t_{dh} | Data hold time | $(t_{cyc} / 2) (\pm) t_{prop}$ | — | — | ns |
| t_{rss} | Register select setup time | $(15 \times t_{cyc} / 2) (\pm) t_{prop}$ | — | — | ns |
| t_{rsh} | Register select hold time | $(t_{cyc} / 2) (\pm) t_{prop}$ | — | — | ns |

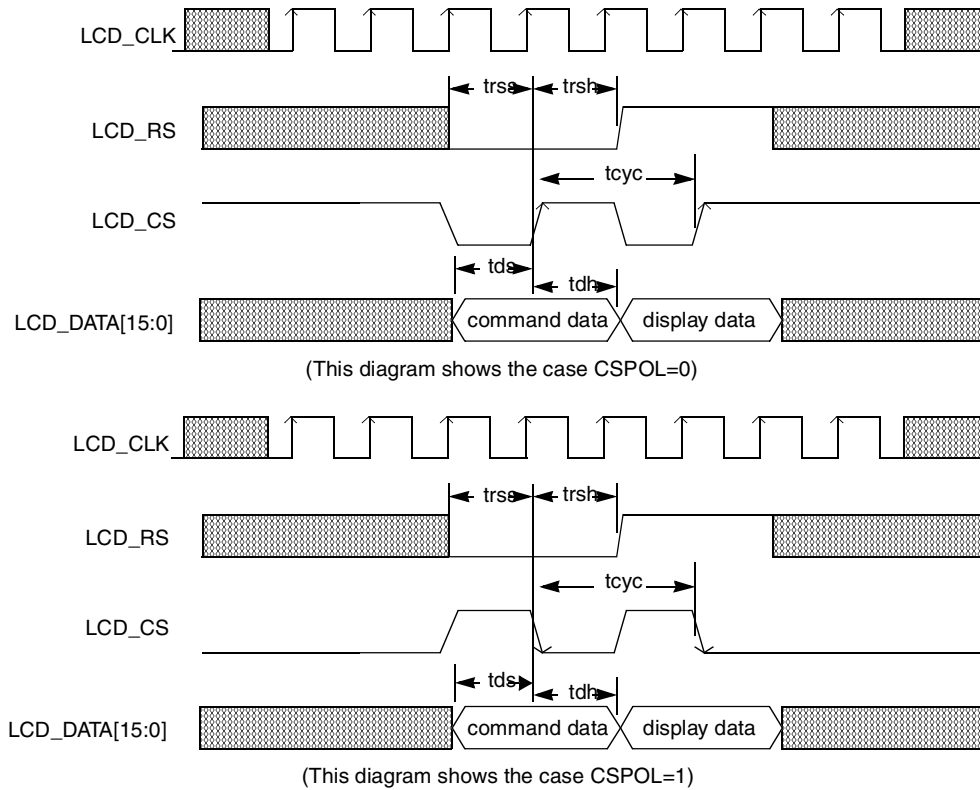


Figure 77. SLCDC Timing Diagram—Parallel Transfers to LCD Device

Table 75. SLCDC Parallel Interface Timing Parameters

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|-----------|----------------------------|--------------------------------|------|------|-------|
| t_{cyc} | Parallel clock cycle time | $78 (\pm) t_{prop}$ | — | 4923 | ns |
| t_{ds} | Data setup time | $(t_{cyc} / 2) (\pm) t_{prop}$ | — | — | — |
| t_{dh} | Data hold time | $(t_{cyc} / 2) (\pm) t_{prop}$ | — | — | — |
| t_{rss} | Register select setup time | $(t_{cyc} / 2) (\pm) t_{prop}$ | — | — | — |
| t_{rsh} | Register select hold time | $(t_{cyc} / 2) (\pm) t_{prop}$ | — | — | — |

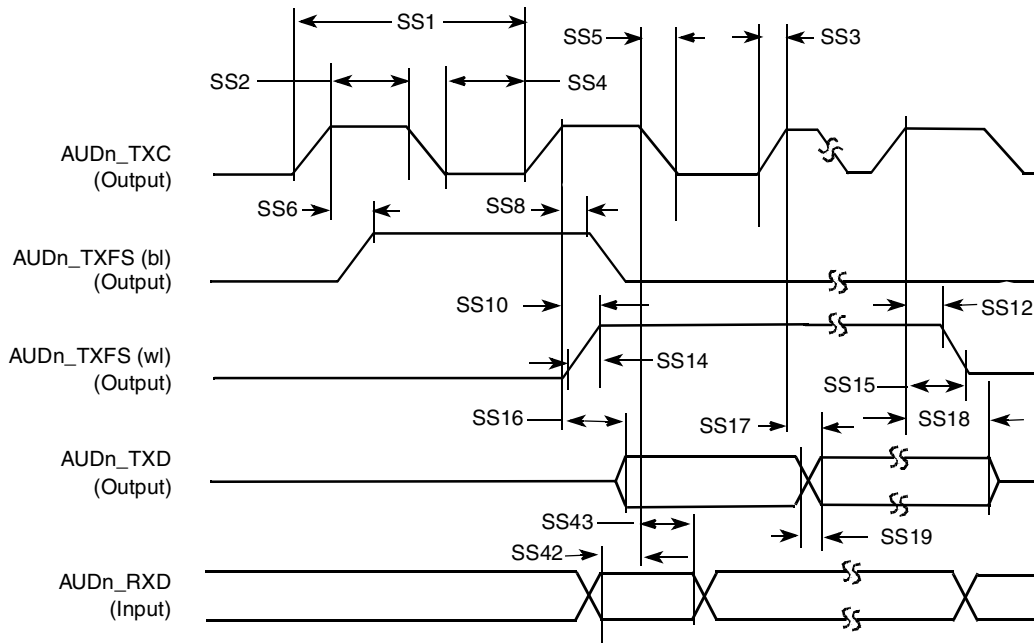
3.6.17 Synchronous Serial Interface (SSI) Timing

The following subsections describe SSI timing in four cases:

- Transmitter with external clock
- Receiver with external clock
- Transmitter with internal clock
- Receiver with internal clock

3.6.17.1 SSI Transmitter Timing with Internal Clock

Figure 78 shows the timing for SSI transmitter with internal clock, and Table 76 describes the timing parameters (SS1–SS52).



Note: SRXD Input in Synchronous mode only

Figure 78. SSI Transmitter with Internal Clock Timing Diagram

Table 76. SSI Transmitter Timing with Internal Clock

| ID | Parameter | Min. | Max. | Unit |
|---|--|------|------|------|
| Internal Clock Operation | | | | |
| SS1 | (Tx/Rx) CK clock period | 81.4 | — | ns |
| SS2 | (Tx/Rx) CK clock high period | 36.0 | — | ns |
| SS3 | (Tx/Rx) CK clock rise time | — | 6.0 | ns |
| SS4 | (Tx/Rx) CK clock low period | 36.0 | — | ns |
| SS5 | (Tx/Rx) CK clock fall time | — | 6.0 | ns |
| SS6 | (Tx) CK high to FS (bl) high | — | 15.0 | ns |
| SS8 | (Tx) CK high to FS (bl) low | — | 15.0 | ns |
| SS10 | (Tx) CK high to FS (wl) high | — | 15.0 | ns |
| SS12 | (Tx) CK high to FS (wl) low | — | 15.0 | ns |
| SS14 | (Tx/Rx) internal FS rise time | — | 6.0 | ns |
| SS15 | (Tx/Rx) internal FS fall time | — | 6.0 | ns |
| SS16 | (Tx) CK high to STXD valid from high impedance | — | 15.0 | ns |
| SS17 | (Tx) CK high to STXD high/low | — | 15.0 | ns |
| SS18 | (Tx) CK high to STXD high impedance | — | 15.0 | ns |
| SS19 | STXD rise/fall time | — | 6.0 | ns |
| Synchronous Internal Clock Operation | | | | |
| SS42 | SRXD setup before (Tx) CK falling | 10.0 | — | ns |
| SS43 | SRXD hold after (Tx) CK falling | 0.0 | — | ns |
| SS52 | Loading | — | 25.0 | pf |

Note:

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on pads when SSI is being used for data transfer.
- "Tx" and "Rx" refer to the transmit and receive sections of the SSI.
- For internal frame sync operation using external clock, the FS timing is the same as that of Tx data (for example, during AC97 mode of operation).

3.6.17.2 SSI Receiver Timing with Internal Clock

Figure 79 shows the timing for the SSI receiver with internal clock. Table 77 describes the timing parameters (SS1–SS51) shown in the figure.

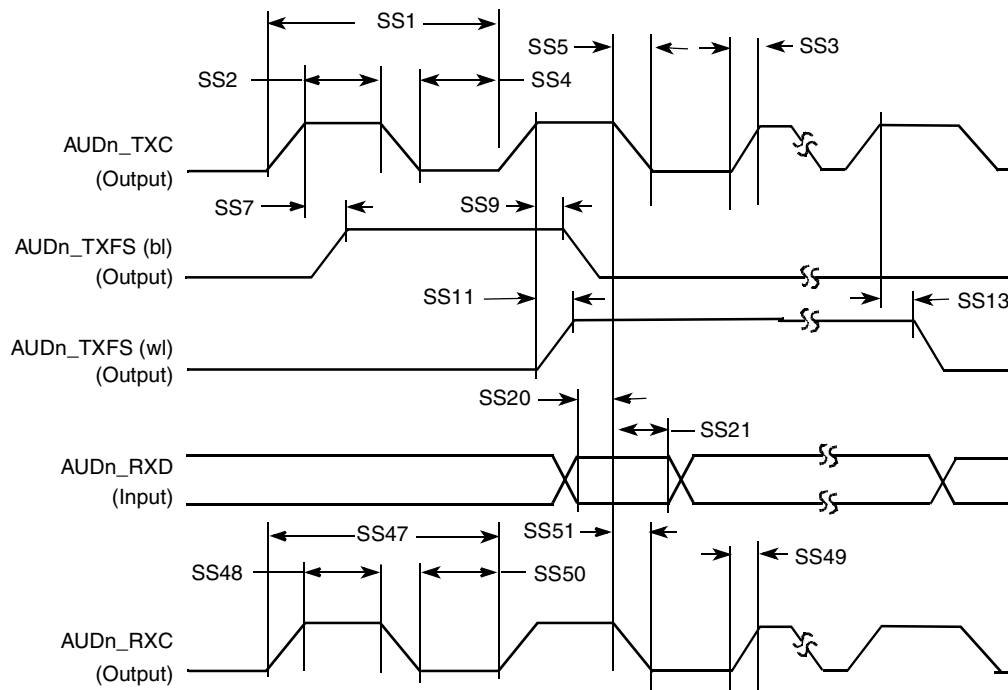


Figure 79. SSI Receiver Internal Clock Timing Diagram

Table 77. SSI Receiver Timing with Internal Clock

| ID | Parameter | Min. | Max. | Unit |
|-------------------------------------|------------------------------------|-------|------|------|
| Internal Clock Operation | | | | |
| SS1 | (Tx/Rx) CK clock period | 81.4 | — | ns |
| SS2 | (Tx/Rx) CK clock high period | 36.0 | — | ns |
| SS3 | (Tx/Rx) CK clock rise time | — | 6.0 | ns |
| SS4 | (Tx/Rx) CK clock low period | 36.0 | — | ns |
| SS5 | (Tx/Rx) CK clock fall time | — | 6.0 | ns |
| SS7 | (Rx) CK high to FS (bl) high | — | 15.0 | ns |
| SS9 | (Rx) CK high to FS (bl) low | — | 15.0 | ns |
| SS11 | (Rx) CK high to FS (wl) high | — | 15.0 | ns |
| SS13 | (Rx) CK high to FS (wl) low | — | 15.0 | ns |
| SS20 | SRXD setup time before (Rx) CK low | 10.0 | — | ns |
| SS21 | SRXD hold time after (Rx) CK low | 0.0 | — | ns |
| Oversampling Clock Operation | | | | |
| SS47 | Oversampling clock period | 15.04 | — | ns |

Table 77. SSI Receiver Timing with Internal Clock (continued)

| ID | Parameter | Min. | Max. | Unit |
|------|--------------------------------|------|------|------|
| SS48 | Oversampling clock high period | 6.0 | — | ns |
| SS49 | Oversampling clock rise time | — | 3.0 | ns |
| SS50 | Oversampling clock low period | 6.0 | — | ns |
| SS51 | Oversampling clock fall time | — | 3.0 | ns |

Note:

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on pads when SSI is being used for data transfer.
- "Tx" and "Rx" refer to the transmit and receive sections of the SSI.
- For internal frame sync operation using external clock, the FS timing is the same as that of Tx Data (for example, during AC97 mode of operation).

3.6.17.3 SSI Transmitter Timing with External Clock

Figure 80 shows the timing for SSI transmitter with external clock. Table 78 describes the timing parameters (SS22-SS46) shown in the figure.

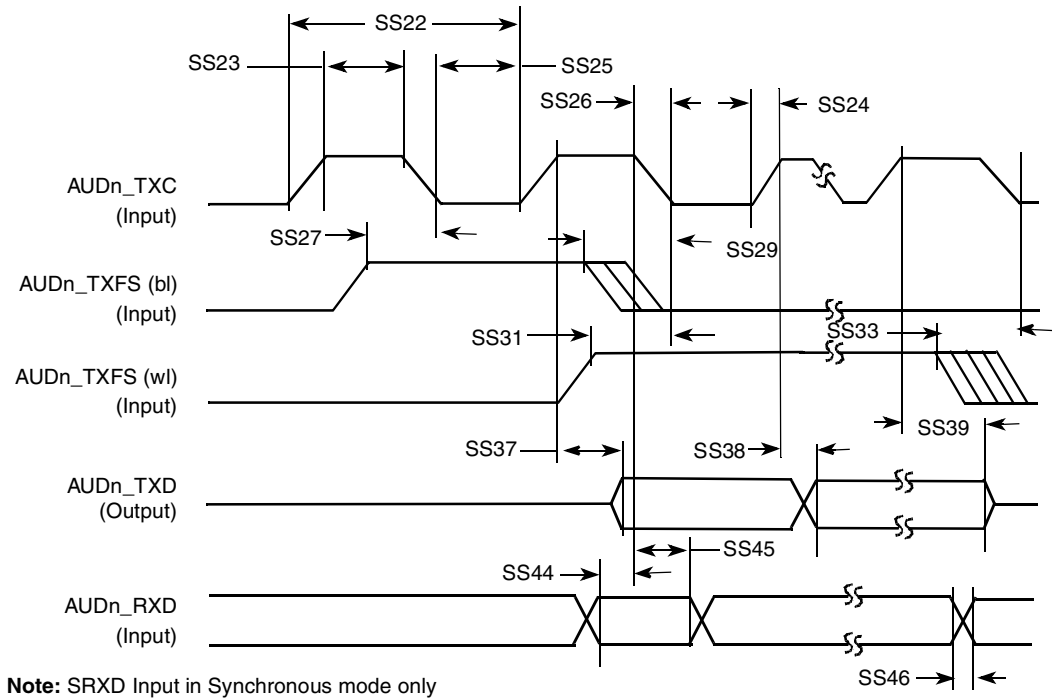


Figure 80. SSI Transmitter with External Clock Timing Diagram

Table 78. SSI Transmitter Timing with External Clock

| ID | Parameter | Min. | Max. | Unit |
|---|--|-------|------|------|
| External Clock Operation | | | | |
| SS22 | (Tx/Rx) CK clock period | 81.4 | — | ns |
| SS23 | (Tx/Rx) CK clock high period | 36.0 | — | ns |
| SS24 | (Tx/Rx) CK clock rise time | — | 6.0 | ns |
| SS25 | (Tx/Rx) CK clock low period | 36.0 | — | ns |
| SS26 | (Tx/Rx) CK clock fall time | — | 6.0 | ns |
| SS27 | FS (bl) low/ high setup before (Tx) CK falling | -10.0 | 15.0 | ns |
| SS29 | FS (bl) low/ high setup before (Tx) CK falling | 10.0 | — | ns |
| SS31 | FS (wl) low/ high setup before (Tx) CK falling | -10.0 | 15.0 | ns |
| SS33 | FS (wl) low/ high setup before (Tx) CK falling | 10.0 | — | ns |
| SS37 | (Tx) CK high to STXD valid from high impedance | — | 15.0 | ns |
| SS38 | (Tx) CK high to STXD high/low | — | 15.0 | ns |
| SS39 | (Tx) CK high to STXD high impedance | — | 15.0 | ns |
| Synchronous External Clock Operation | | | | |
| SS44 | SRXD setup before (Tx) CK falling | 10.0 | — | ns |
| SS45 | SRXD hold after (Tx) CK falling | 2.0 | — | ns |
| SS46 | SRXD rise/fall time | — | 6.0 | ns |

Note:

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on pads when SSI is being used for data transfer.
- "Tx" and "Rx" refer to the transmit and receive sections of the SSI.
- For internal frame sync operation using external clock, the FS timing is the same as that of Tx data (for example, during AC97 mode of operation).

3.6.17.4 SSI Receiver Timing with External Clock

Figure 81 shows the timing for SSI receiver with external clock. Table 79 describes the timing parameters (SS22–SS41) used in the figure.

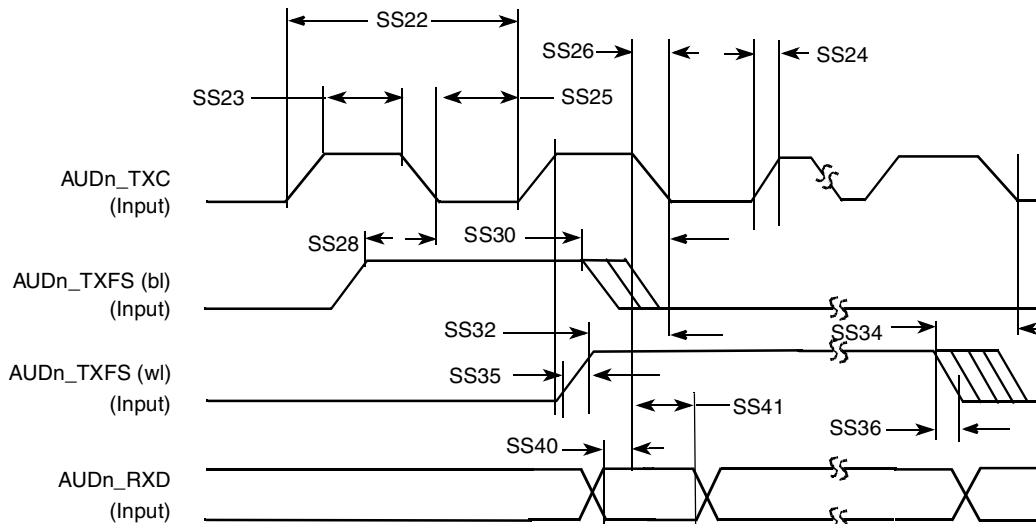


Figure 81. SSI Receiver with External Clock Timing Diagram

Table 79. SSI Receiver Timing with External Clock

| ID | Parameter | Min. | Max. | Unit |
|---------------------------------|--|-------|------|------|
| External Clock Operation | | | | |
| SS22 | (Tx/Rx) CK clock period | 81.4 | — | ns |
| SS23 | (Tx/Rx) CK clock high period | 36.0 | — | ns |
| SS24 | (Tx/Rx) CK clock rise time | — | 6.0 | ns |
| SS25 | (Tx/Rx) CK clock low period | 36.0 | — | ns |
| SS26 | (Tx/Rx) CK clock fall time | — | 6.0 | ns |
| SS28 | FS (bl) low/ high setup before (Tx) CK falling | -10.0 | 15.0 | ns |
| SS30 | FS (bl) low/ high setup before (Tx) CK falling | 10.0 | — | ns |
| SS32 | FS (wl) low/ high setup before (Tx) CK falling | -10.0 | 15.0 | ns |
| SS34 | FS (wl) low/ high setup before (Tx) CK falling | 10.0 | — | ns |
| SS35 | (Tx/Rx) External FS rise time | — | 6.0 | ns |
| SS36 | (Tx/Rx) External FS fall time | — | 6.0 | ns |
| SS40 | SRXD setup time before (Rx) CK low | 10.0 | — | ns |
| SS41 | SRXD hold time after (Rx) CK low | 2.0 | — | ns |

Note:

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on pads when SSI is being used for data transfer.

- "Tx" and "Rx" refer to the transmit and receive sections of the SSI.
- For internal frame sync operation using external clock, the FS timing is the same as that of Tx data (for example, during AC97 mode of operation).

3.6.18 Touchscreen ADC Electrical Specifications and Timing

This section describe the electrical specifications, operation modes, and timing of the touchscreen ADC.

3.6.18.1 ADC Electrical Specifications

Table 80 shows the electrical specifications for the touchscreen ADC.

Table 80. Touchscreen ADC Electrical Specifications

| Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--|---------------------------------|------|------|------|------------|
| ADC | | | | | |
| Input sampling capacitance (C_S) | No pin/pad capacitance included | — | 2 | — | pF |
| Resolution | — | 12 | | | bits |
| Analog Bias | | | | | |
| Resistance value between <i>ref</i> and <i>agndref</i> | — | — | 1.6 | — | k Ω |
| Timing Characteristics | | | | | |
| Maximum sampling rate (fs) | — | 125 | — | — | kHz |
| Maximum input clock frequency (fclk) | — | 1.75 | — | — | MHz |
| Clock duty cycle | — | 45 | 50 | 55 | % |
| Multiplexed inputs | — | 8 | | | — |
| Data latency | — | 12.5 | | | clk cycles |
| Power-up time ¹ | — | 14 | | | clk cycles |
| clk falling edge to sampling delay (tsd) | — | 2 | 5 | 8 | ns |
| soc input setup time before clk rising edge (tsocst) | — | 0.5 | 1 | 3 | ns |
| soc input hold time after clk rising edge (tsochld) | — | 2 | 3 | 6 | ns |
| eoc delay after clk rise edge (teoc) | With a 250fF load | 2 | 7 | 10 | ns |
| Valid data out delay after eoc rise edge (tdata) | With a 250fF load | 5 | 8 | 13 | ns |

Table 80. Touchscreen ADC Electrical Specifications (continued)

| Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--|----------------------|------|---------|------------|----------|
| Power Supply Requirements | | | | | |
| Current consumption ² NVCC_ADC QV _{DD} | — | — | — | 2.1 0.5 | mA mA |
| Power-down current NVCC_ADC QV _{DD} | — | — | — | 1 10 | μA μA |
| Touchscreen Interface | | | | | |
| Expected plate resistance | — | 100 | — | 1500 | Ω |
| Switch drivers on resistance | GND and VDD switches | — | — | 10 | Ω |
| Conversion Characteristics³ | | | | | |
| DNL ⁴ | fin = 1 kHz | — | +/-0.75 | — | LSB |
| INL ⁴ | fin = 1 kHz | — | +/-2.0 | — | LSB |
| Gain + Offset Error | — | — | — | +/-2 | %FS |

¹ This comprises only the required initial dummy conversion cycle. Additional power-up time depends on the *enadc*, *reset* and *soc* signals applied to the touchscreen controller.

² This value only includes the ADC and the driver switches, but it does not take into account the current consumption in the touchscreen plate. For example, if the plate resistance is 100 W, the total current consumption is about 33 mA.

³ At avdd = 3.3 V, dvdd = 1.2 V, Tjunction = 50 °C, fclk = 1.75 MHz, any process corner, unless otherwise noted

⁴ Value measured with a -0.5 dBFS sinusoidal input signal and computed with the code density test.

3.6.18.2 ADC Timing Diagrams

Figure 82 represents the synchronization between the signals *clk*, *soc*, *eoc*, and the output bits in the usage of the internal ADC. After a conversion cycle *eoc* is asserted, a new conversion begins only when the assertion of *soc* is detected. Thus if the *soc* signal is continuously asserted, the ADC undergoes successive conversion cycles and achieves the maximum sampling rate. If *soc* is negated, no conversion is initiated.

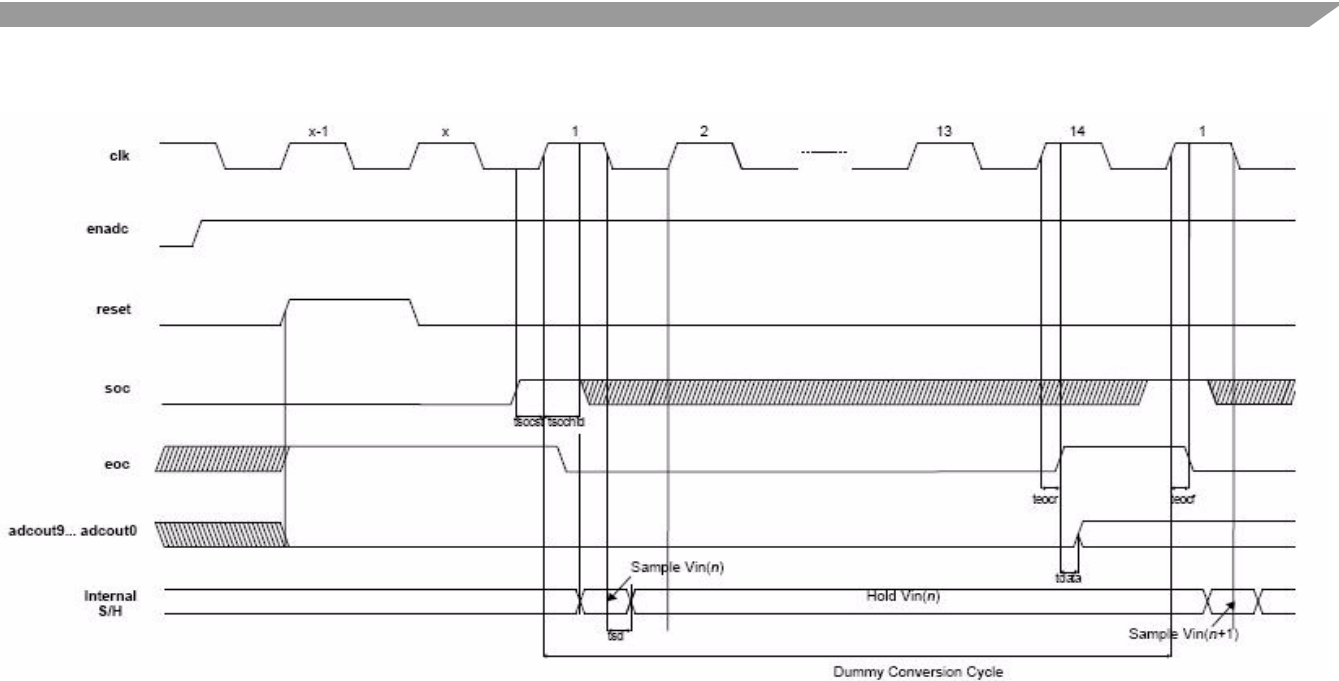


Figure 82. Startup Sequence

The output data can be read from *adcout11...adcout0*, and is available *tdata* nanoseconds after the rising edge of *eoc*. The *reset* signal and the digital signals controlling the analog switches (*ypsw*, *xpsw*, *ynsw*, *xnsw*) are totally asynchronous.

The following conditions are necessary to guarantee the correct operation of the ADC:

- The input multiplexer selection (*selin11...selin0*) is stable during both the last clock cycle (14th) and the first clock cycle (1st). The best way to guarantee this is to make the input multiplexer selection during clock cycles 2 to 13.
- The references are stable during clock cycle 1 to 13. The best way to guarantee this is to make the reference multiplexer selection (*selrefp* and *selrefn*) before issuing an *soc* pulse and changing it only after an *eoc* pulse has been acquired, during the last clock cycle (14).

Figure 83 shows the timing for ADC normal operation.

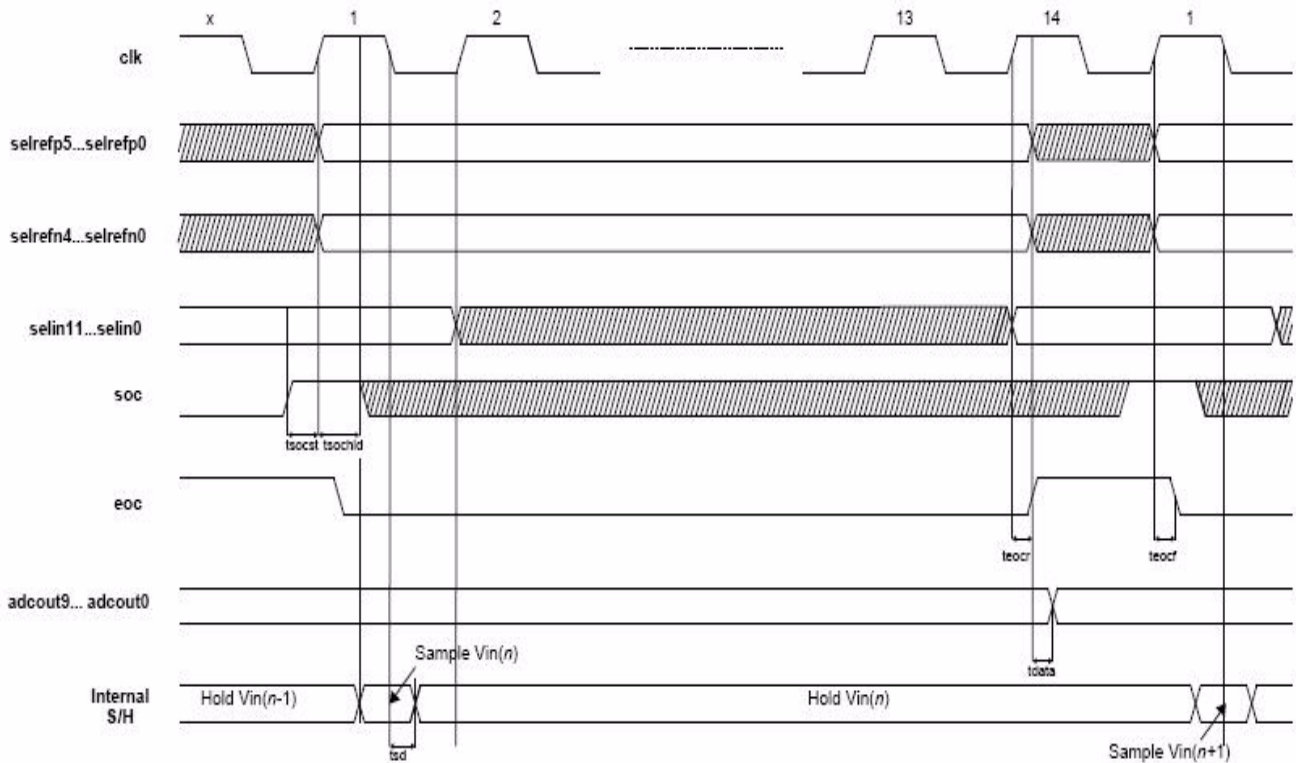


Figure 83. Timing for ADC Normal Operation

When the ADC is used so that the idle clock cycles occur between conversions (due to the negation of *soc*), the *selin* inputs must be stable at least 1 clock cycle before the clock's rising edge where the *soc* signal is latched. Also, *selrefp* and *selrefn* must be stable by the time the *soc* signal is latched. These conditions are met if *enadc*=1 and *reset*=0 throughout ADC operation, including the idle cycles. If the conditions are not met, or if power is lost during ADC operation, then a new startup sequence is required for ADC to become operational again.

Figure 84 represents the usage of the ADC with idle cycles between conversions. This diagram is valid for any value of N equal or greater than 1.

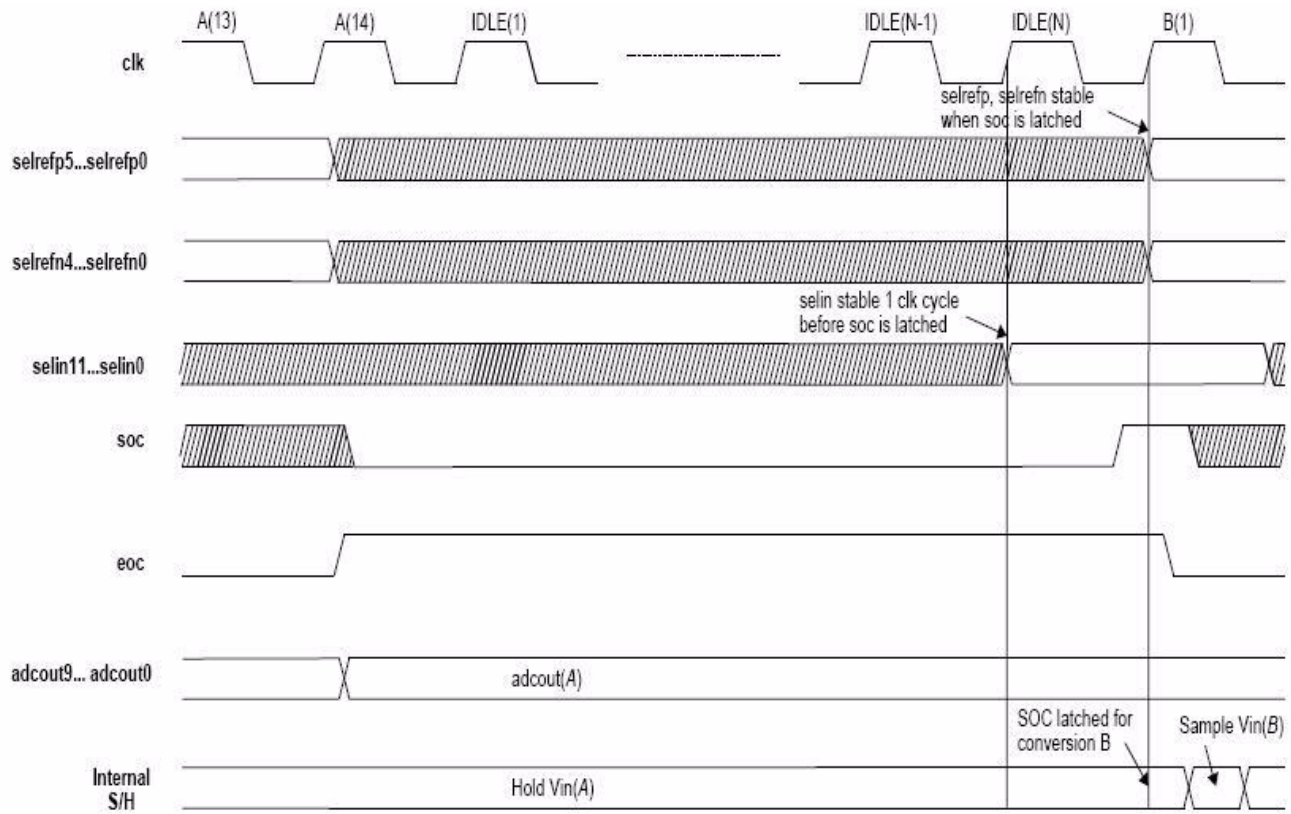


Figure 84. ADC Usage with Idle Cycles Between Conversions

3.6.19 UART Timing

This section describes the timing of the UART module in serial and parallel mode.

3.6.19.1 UART RS-232 Serial Mode Timing

3.6.19.1.1 UART Transmit Timing in RS-232 Serial Mode

Figure 85 shows the UART transmit timing in RS-232 serial mode, showing only 8 data bits and 1 stop bit. Table 81 describes the timing parameter (UA1) shown in the figure.

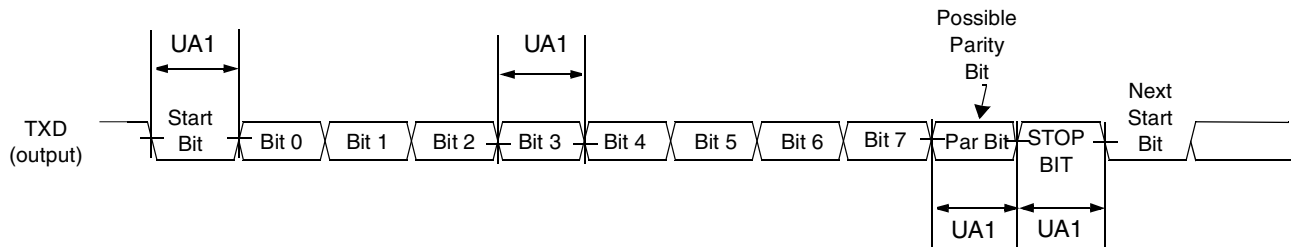


Figure 85. UART RS-232 Serial Mode Transmit Timing Diagram

Table 81. UART RS-232 Serial Mode Transmit Timing Parameters

| ID | Parameter | Symbol | Min. | Max. | Units |
|-----|-------------------|------------|---------------------------------------|-----------------------------------|-------|
| UA1 | Transmit Bit Time | t_{Tbit} | $1/F_{baud_rate}^1 - T_{ref_clk}^2$ | $1/F_{baud_rate} + T_{ref_clk}$ | — |

¹ F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is $(ipg_perclk \text{ frequency})/16$.

² T_{ref_clk} : The period of UART reference clock ref_clk (ipg_perclk after RFDIV divider).

3.6.19.1.2 UART Receive Timing in RS-232 Serial Mode

Figure 86 shows the UART receive timing in RS-232 serial mode, showing only 8 data bits and 1 stop bit. Table 82 describes the timing parameter (UA2) shown in the figure.

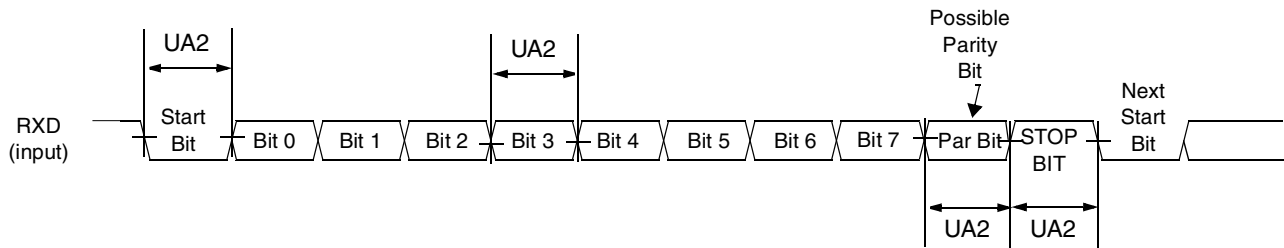


Figure 86. UART RS-232 Serial Mode Receive Timing Diagram

Table 82. UART RS-232 Serial Mode Receive Timing Parameters

| ID | Parameter | Symbol | Min. | Max. | Units |
|-----|-------------------------------|------------|---|---|-------|
| UA2 | Receive bit time ¹ | t_{Rbit} | $1/F_{baud_rate}^2 - 1/(16 \times F_{baud_rate})$ | $1/F_{baud_rate} + 1/(16 \times F_{baud_rate})$ | — |

¹ Note: The UART receiver can tolerate $1/(16 \times F_{baud_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud_rate})$.

² F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is $(ipg_perclk \text{ frequency})/16$.

3.6.19.2 UART Infrared (IrDA) Mode Timing

The following subsections describe the UART transmit and receive timing in IrDA mode.

3.6.19.2.3 UART IrDA Mode Transmit Timing

Figure 87 depicts the UART transmit timing in IrDA mode, showing only 8 data bits and 1 stop bit. Table 83 describes the timing parameters (UA3–UA4) shown in the figure.

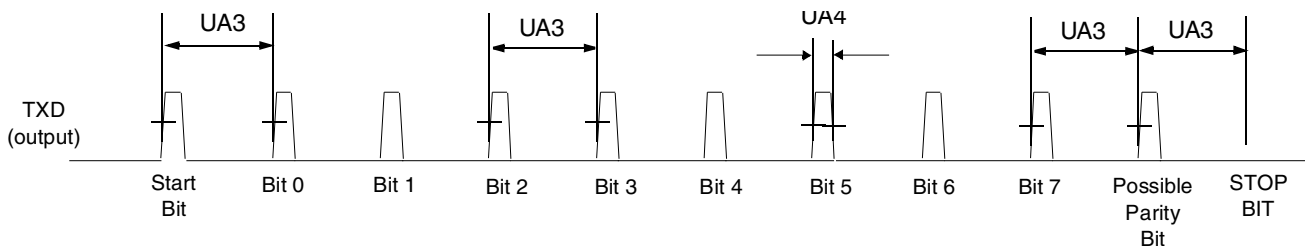


Figure 87. UART IrDA Mode Transmit Timing Diagram

Table 83. UART IrDA Mode Transmit Timing Parameters

| ID | Parameter | Symbol | Min. | Max. | Units |
|-----|--------------------------------|----------------|---|---|-------|
| UA3 | Transmit bit time in IrDA mode | t_{TIRbit} | $1/F_{baud_rate}^1 - T_{ref_clk}^2$ | $1/F_{baud_rate} + T_{ref_clk}$ | — |
| UA4 | Transmit IR pulse duration | $t_{TIRpulse}$ | $(3/16) \times (1/F_{baud_rate}) - T_{ref_clk}$ | $(3/16) \times (1/F_{baud_rate}) + T_{ref_clk}$ | — |

¹ F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is $(ipg_perclk \text{ frequency})/16$.

² T_{ref_clk} : The period of UART reference clock ref_clk (ipg_perclk after RFDIV divider).

3.6.19.2.4 UART IrDA Mode Receive Timing

Figure 88 shows the UART receive timing for IrDA mode, for a format of 8 data bits and 1 stop bit. Table 84 describes the timing parameters (UA5–UA6) shown in the figure.

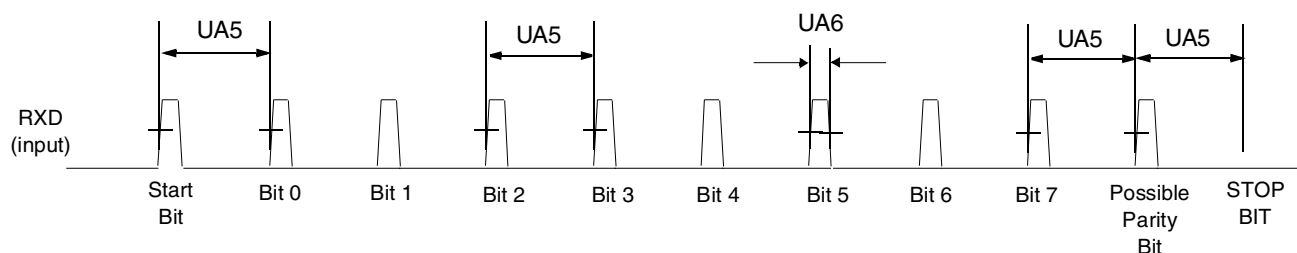


Figure 88. UART IrDA Mode Receive Timing Diagram

Table 84. UART IrDA Mode Receive Timing Parameters

| ID | Parameter | Symbol | Min. | Max. | Units |
|-----|--|----------------|---|---|-------|
| UA5 | Receive bit time ¹ in IrDA mode | t_{RIRbit} | $1/F_{baud_rate}^2 - 1/(16 \times F_{baud_rate})$ | $1/F_{baud_rate} + 1/(16 \times F_{baud_rate})$ | — |
| UA6 | Receive IR pulse duration | $t_{RIRpulse}$ | 1.41 us | $(5/16) \times (1/F_{baud_rate})$ | — |

¹ Note: The UART receiver can tolerate $1/(16 \times F_{baud_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud_rate})$.

² F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is $(ipg_perclk \text{ frequency})/16$.

3.6.20 USBOTG Timing

This section describes timing for the USB OTG port and host ports. Both serial and parallel interfaces are described.

3.6.20.1 USB Serial Interface Timing

The USB serial transceiver is configurable to four modes supporting four different serial interfaces:

- DAT_SE0 bidirectional, 3-wire mode
- DAT_SE0 unidirectional, 6-wire mode
- VP_VM bidirectional, 4-wire mode
- VP_VM unidirectional, 6-wire mode

The following subsections describe the timings for these four modes.

3.6.20.1.1 DAT_SE0 Bidirectional Mode Timing

Table 85 defines the DAT_SE0 bidirectional mode signals.

Table 85. Signal Definitions—DAT_SE0 Bidirectional Mode

| Name | Direction | Signal Description |
|------------|-----------|--|
| USB_TXOE_B | Out | Transmit enable, active low |
| USB_DAT_VP | Out In | Tx data when USB_TXOE_B is low Differential Rx data when USB_TXOE_B is high |
| USB_SE0_VM | Out In | SE0 drive when USB_TXOE_B is low SE0 Rx indicator when USB_TXOE_B is high |

Figure 89 shows the USB transmit waveform in DAT_SE0 bidirectional mode diagram.

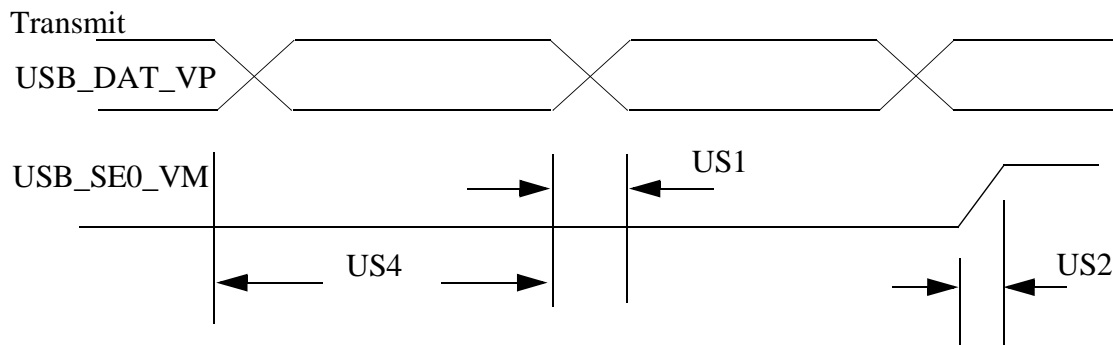


Figure 89. USB Transmit Waveform in DAT_SE0 Bidirectional Mode

Figure 90 shows the USB receive waveform in DAT_SE0 bidirectional mode diagram.

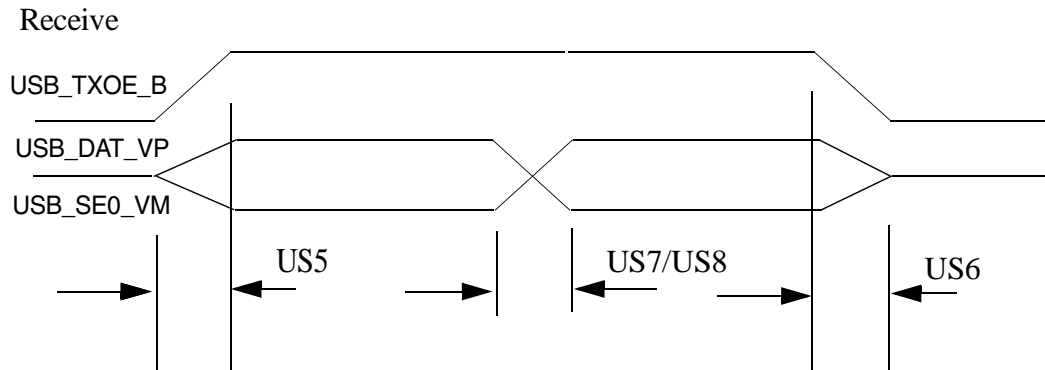


Figure 90. USB Receive Waveform in DAT_SE0 Bidirectional Mode

Table 86 shows the OTG port timing specification in DAT_SE0 bidirectional mode.

Table 86. OTG Port Timing Specification in DAT_SE0 Bidirectional Mode

| No. | Parameter | Signal Name | Direction | Min. | Max. | Unit | Conditions/ Reference Signal |
|-----|-------------------|--------------------------|-----------|------|------|------|---------------------------------|
| US1 | Tx rise/fall time | USB_DAT_VP | Out | — | 5.0 | ns | 50 pF |
| US2 | Tx rise/fall time | USB_SE0_VM | Out | — | 5.0 | ns | 50 pF |
| US3 | Tx rise/fall time | USB_TXOE_B | Out | — | 5.0 | ns | 50 pF |
| US4 | Tx duty cycle | USB_DAT_VP | Out | 49.0 | 51.0 | % | — |
| US5 | Enable Delay | USB_DAT_VP USB_SE0_VM | In | — | 8.0 | ns | USB_TXOE_B |
| US6 | Disable Delay | USB_DAT_VP USB_SE0_VM | In | — | 10.0 | ns | USB_TXOE_B |
| US7 | Rx rise/fall time | USB_DAT_VP | In | — | 3.0 | ns | 35 pF |
| US8 | Rx rise/fall time | USB_SE0_VM | In | — | 3.0 | ns | 35 pF |

3.6.20.1.2 DAT_SE0 Unidirectional Mode Timing

Table 87 defines the DAT_SE0 unidirectional mode signals.

Table 87. Signal Definitions—DAT_SE0 Unidirectional Mode

| Name | Direction | Signal Description |
|------------|-----------|--|
| USB_TXOE_B | Out | Transmit enable, active low |
| USB_DAT_VP | Out | Tx data when USB_TXOE_B is low |
| USB_SE0_VM | Out | SE0 drive when USB_TXOE_B is low |
| USB_VP1 | In | Buffered data on DP when USB_TXOE_B is high |
| USB_VM1 | In | Buffered data on DM when USB_TXOE_B is high |
| USB_RCV | In | Differential Rx data when USB_TXOE_B is high |

Figure 91 shows the USB transmit waveform in DAT_SE0 unidirectional mode diagram.

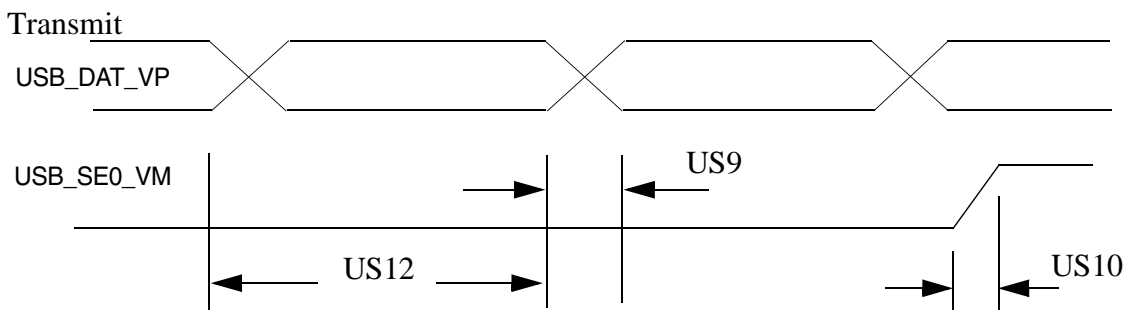


Figure 91. USB Transmit Waveform in DAT_SE0 Unidirectional Mode

Figure 92 shows the USB receive waveform in DAT_SE0 unidirectional mode diagram.

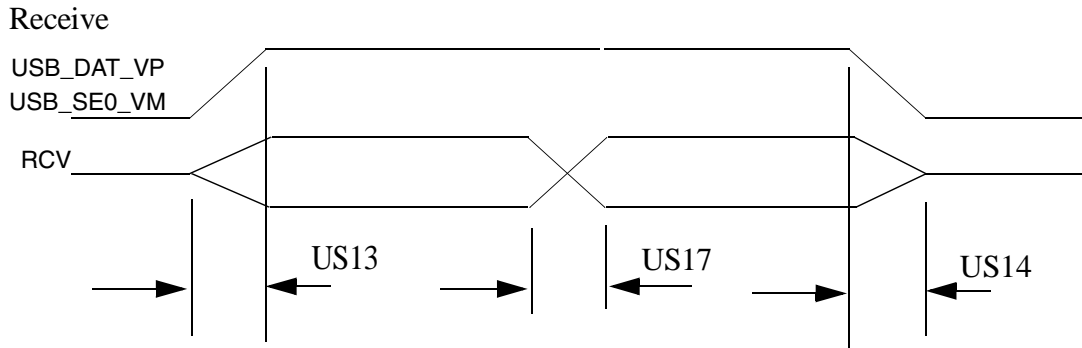


Figure 92. USB Receive Waveform in DAT_SE0 Unidirectional Mode

Table 88 shows the USB port timing specification in DAT_SE0 unidirectional mode.

Table 88. USB Port Timing Specification in DAT_SE0 Unidirectional Mode

| No. | Parameter | Signal Name | Signal Source | Min. | Max. | Unit | Condition/Reference Signal |
|------|-------------------|--------------------------|---------------|------|------|------|----------------------------|
| US9 | Tx rise/fall time | USB_DAT_VP | Out | — | 5.0 | ns | 50 pF |
| US10 | Tx rise/fall time | USB_SE0_VM | Out | — | 5.0 | ns | 50 pF |
| US11 | Tx rise/fall time | USB_TXOE_B | Out | — | 5.0 | ns | 50 pF |
| US12 | Tx duty cycle | USB_DAT_VP | Out | 49.0 | 51.0 | % | — |
| US13 | Enable Delay | USB_DAT_VP USB_SE0_VM | In | — | 8.0 | ns | USB_TXOE_B |
| US14 | Disable Delay | USB_DAT_VP USB_SE0_VM | In | — | 10.0 | ns | USB_TXOE_B |
| US15 | Rx rise/fall time | USB_VP1 | In | — | 3.0 | ns | 35 pF |
| US16 | Rx rise/fall time | USB_VM1 | In | — | 3.0 | ns | 35 pF |
| US17 | Rx rise/fall time | USB_RCV | In | — | 3.0 | ns | 35 pF |

3.6.20.1.3 VP_VM Bidirectional Mode Timing

Table 89 defines the VP_VM bidirectional mode signals.

Table 89. Signal Definitions—VP_VM Bidirectional Mode

| Name | Direction | Signal Description |
|------------|---------------------|---|
| USB_TXOE_B | Out | <ul style="list-style-type: none"> Transmit enable, active low |
| USB_DAT_VP | Out (Tx) In (Rx) | <ul style="list-style-type: none"> Tx VP data when USB_TXOE_B is low Rx VP data when USB_TXOE_B is high |
| USB_SE0_VM | Out (Tx) In (Rx) | <ul style="list-style-type: none"> Tx VM data when USB_TXOE_B low Rx VM data when USB_TXOE_B high |
| USB_RCV | In | <ul style="list-style-type: none"> Differential Rx data |

Figure 93 shows the USB transmit waveform in VP_VM bidirectional mode diagram.

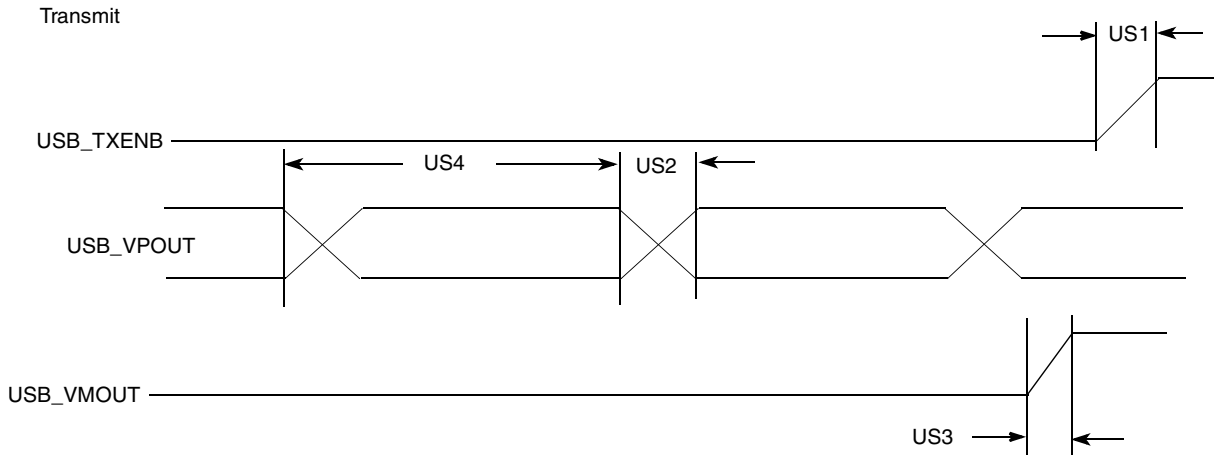


Figure 93. USB Transmit Waveform in VP_VM Bidirectional Mode

Figure 94 shows the USB receive waveform in VP_VM bidirectional mode diagram.

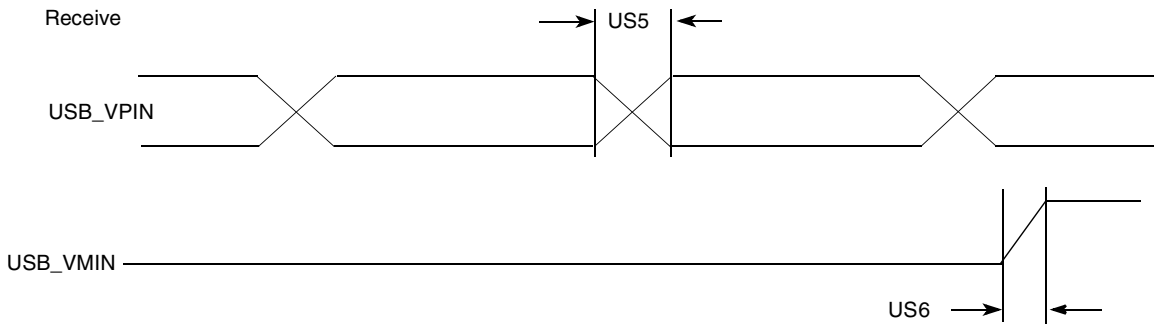


Figure 94. USB Receive Waveform in VP_VM Bidirectional Mode

Table 90 shows the USB port timing specification in VP_VM bidirectional mode.

Table 90. USB Port Timing Specifications in VP_VM Bidirectional Mode

| No. | Parameter | Signal Name | Direction | Min. | Max. | Unit | Condition/ Reference Signal |
|------|-------------------|--------------------------|-----------|------|------|------|--------------------------------|
| US18 | Tx rise/fall time | USB_DAT_VP | Out | — | 5.0 | ns | 50 pF |
| US19 | Tx rise/fall time | USB_SE0_VM | Out | — | 5.0 | ns | 50 pF |
| US20 | Tx rise/fall time | USB_TXOE_B | Out | — | 5.0 | ns | 50 pF |
| US21 | Tx duty cycle | USB_DAT_VP | Out | 49.0 | 51.0 | % | — |
| US22 | Tx high overlap | USB_SE0_VM | Out | 0.0 | — | ns | USB_DAT_VP |
| US23 | Tx low overlap | USB_SE0_VM | Out | — | 0.0 | ns | USB_DAT_VP |
| US24 | Enable delay | USB_DAT_VP USB_SE0_VM | In | — | 8.0 | ns | USB_TXOE_B |
| US25 | Disable delay | USB_DAT_VP USB_SE0_VM | In | — | 10.0 | ns | USB_TXOE_B |

Table 90. USB Port Timing Specifications in VP_VM Bidirectional Mode (continued)

| No. | Parameter | Signal Name | Direction | Min. | Max. | Unit | Condition/ Reference Signal |
|------|-------------------|-------------|-----------|------|------|------|--------------------------------|
| US26 | Rx rise/fall time | USB_DAT_VP | In | — | 3.0 | ns | 35 pF |
| US27 | Rx rise/fall time | USB_SE0_VM | In | — | 3.0 | ns | 35 pF |
| US28 | Rx skew | USB_DAT_VP | Out | -4.0 | +4.0 | ns | USB_SE0_VM |
| US29 | Rx skew | USB_RCV | Out | -6.0 | +2.0 | ns | USB_DAT_VP |

3.6.20.1.4 VP_VM Unidirectional Mode Timing

Table 91 defines the signals for USB in VP_VM unidirectional mode.

Table 91. Signal Definitions for USB VP_VM Unidirectional Mode

| Name | Direction | Signal Description |
|------------|-----------|------------------------------------|
| USB_TXOE_B | Out | Transmit enable, active low |
| USB_DAT_VP | Out | Tx VP data when USB_TXOE_B is low |
| USB_SE0_VM | Out | Tx VM data when USB_TXOE_B is low |
| USB_VP1 | In | Rx VP data when USB_TXOE_B is high |
| USB_VM1 | In | Rx VM data when USB_TXOE_B is high |
| USB_RCV | In | Differential Rx data |

Figure 95 shows the USB transmit waveform in VP_VM unidirectional mode diagram.

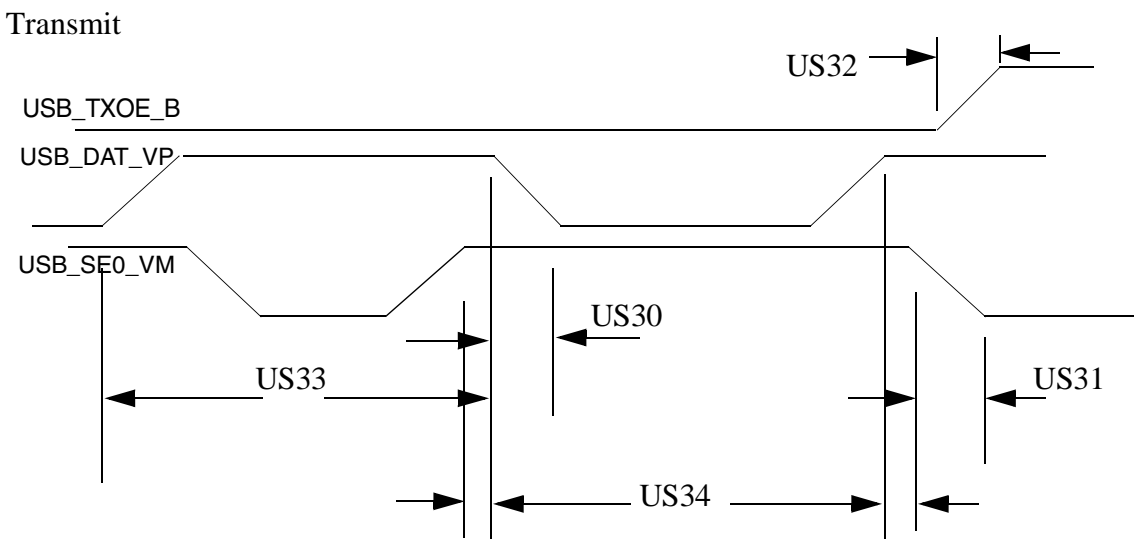


Figure 95. USB Transmit Waveform in VP_VM Unidirectional Mode

Figure 96 shows the USB receive waveform in VP_VM unidirectional mode diagram.

Receive

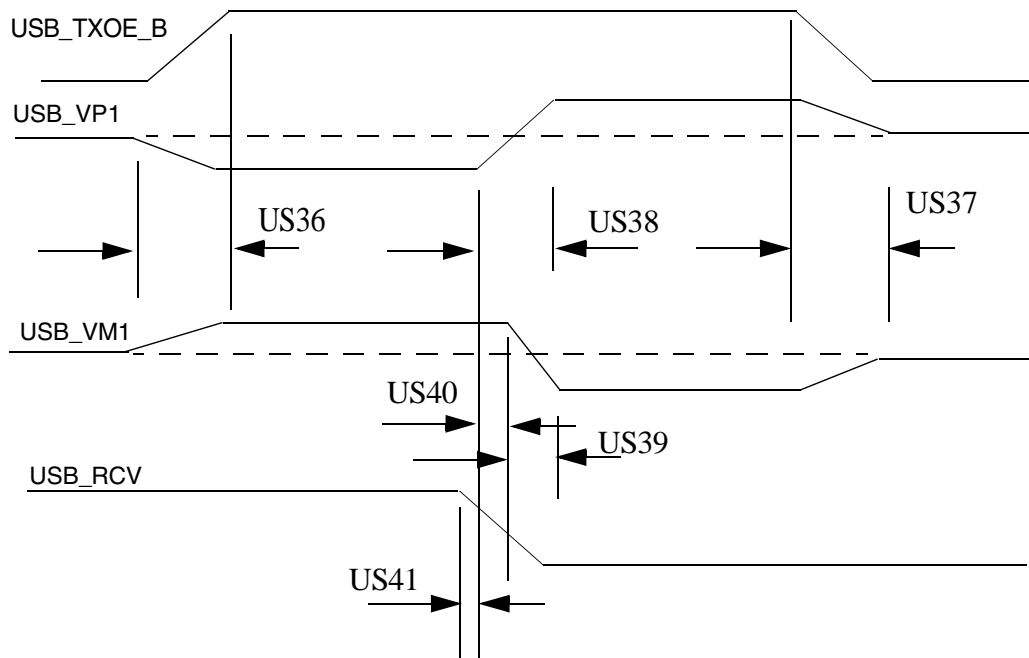


Figure 96. USB Receive Waveform in VP_VM Unidirectional Mode

Table 92 shows the timing specifications for USB in VP_VM unidirectional mode.

Table 92. USB Timing Specifications in VP_VM Unidirectional Mode

| No. | Parameter | Signal | Direction | Min. | Max. | Unit | Conditions/ Reference Signal |
|------|-------------------|--------------------------|-----------|------|------|------|---------------------------------|
| US30 | Tx rise/fall time | USB_DAT_VP | Out | — | 5.0 | ns | 50 pF |
| US31 | Tx rise/fall time | USB_SE0_VM | Out | — | 5.0 | ns | 50 pF |
| US32 | Tx rise/fall time | USB_TXOE_B | Out | — | 5.0 | ns | 50 pF |
| US33 | Tx duty cycle | USB_DAT_VP | Out | 49.0 | 51.0 | % | — |
| US34 | Tx high overlap | USB_SE0_VM | Out | 0.0 | — | ns | USB_DAT_VP |
| US35 | Tx low overlap | USB_SE0_VM | Out | — | 0.0 | ns | USB_DAT_VP |
| US36 | Enable delay | USB_DAT_VP USB_SE0_VM | In | — | 8.0 | ns | USB_TXOE_B |
| US37 | Disable delay | USB_DAT_VP USB_SE0_VM | In | — | 10.0 | ns | USB_TXOE_B |
| US38 | Rx rise/fall time | USB_VP1 | In | — | 3.0 | ns | 35 pF |
| US39 | Rx rise/fall time | USB_VM1 | In | — | 3.0 | ns | 35 pF |
| US40 | Rx skew | USB_VP1 | Out | -4.0 | +4.0 | ns | USB_SE0_VM |
| US41 | Rx skew | USB_RCV | Out | -6.0 | +2.0 | ns | USB_DAT_VP |

3.6.20.2 USB Parallel Interface Timing

Table 93 defines the USB parallel interface signals.

Table 93. Signal Definitions for USB Parallel Interface

| Name | Direction | Signal Description |
|---------------|-----------|---|
| USB_Clk | In | Interface clock - all interface signals are synchronous to USB_Clk |
| USB_Data[7:0] | I/O | Bidirectional data bus, driven low by the link during idle - bus ownership is determined by the direction |
| USB_Dir | In | Direction - control the direction of the data bus |
| USB_Stp | Out | Stop - the link asserts this signal for one clock cycle to stop the data stream currently on the bus |
| USB_Nxt | In | Next - the PHY asserts this signal to throttle the data |

Figure 97 shows the USB parallel mode transmit/receive waveform. Table 94 describes the timing parameters (USB15–USB17) shown in the figure.

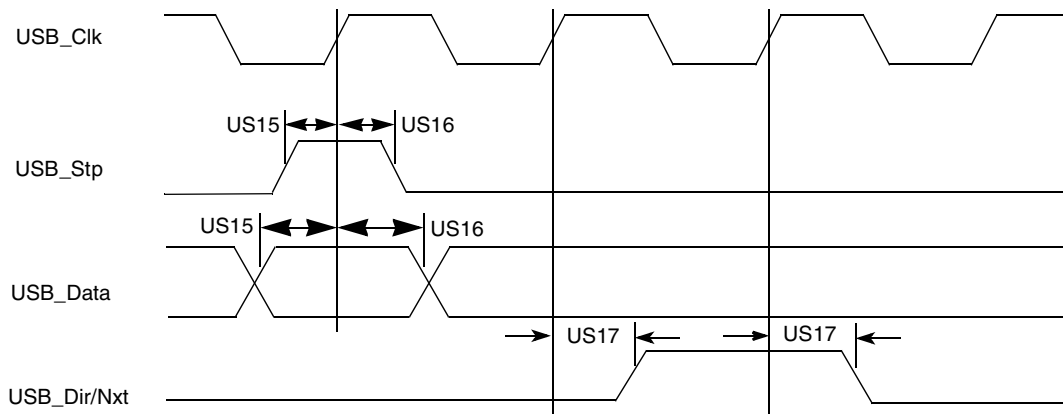


Figure 97. USB Parallel Mode Transmit/Receive Waveform

Table 94. USB Timing Specification in Parallel Mode

| ID | Parameter | Min. | Max. | Unit | Conditions/ Reference Signal |
|------|---------------------------------------|------|------|------|---------------------------------|
| US15 | Setup time (Dir&Nxt in, Data in) | — | 6.0 | ns | 10 pF |
| US16 | Hold time (Dir&Nxt in, Data in) | — | 0.0 | ns | 10 pF |
| US17 | Output delay time (Stp out, Data out) | — | 9.0 | ns | 10 pF |

4 Package Information and Contact Assignment

4.1 400 MAPBGA—Case 17x17 mm, 0.8 mm Pitch

Figure 98 shows the i.MX25 production package. The following notes apply to Figure 98:

- All dimensions in millimeters.
- Dimensioning and tolerancing per ASME Y14.5M-1994.

- Maximum solder bump diameter measured parallel to datum A.
- Datum A, the seating plane, is determined by the spherical crowns of the solder bumps.
- Parallelism measurement shall exclude any effect of mark on top surface of package.

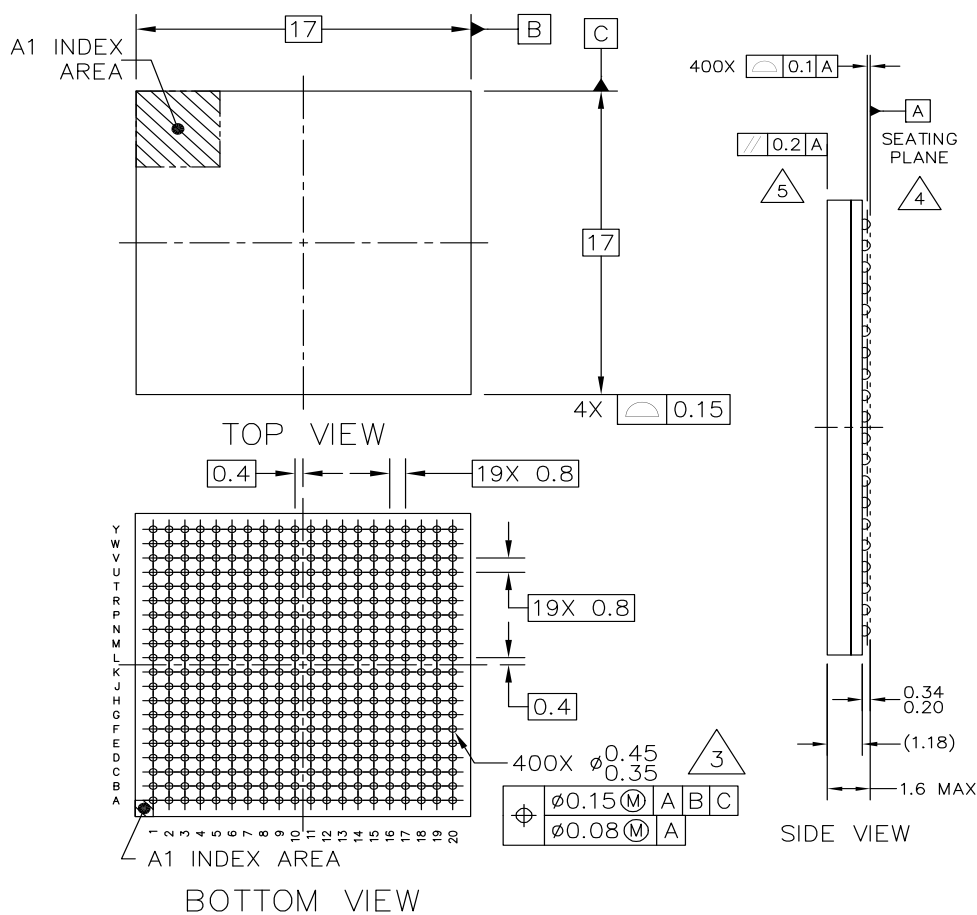


Figure 98. i.MX25 Production Package

4.2 Ground, Power, Sense, and Reference Contact Assignments

Figure 95 shows ground, power, sense, and reference contact assignments.

Table 95. Ground, Power Sense, and Reference Contact Assignments

| Contact Name | Contact Assignment |
|--------------|--------------------|
| BATT_VDD | P10 |
| FUSE_VDD | T17 |
| MPLL_GND | U17 |
| MPLL_VDD | U18 |
| NGND_ADC | Y13 |
| NVCC_ADC | W13 |
| NVCC_CRM | N14 |

Table 95. Ground, Power Sense, and Reference Contact Assignments (continued)

| Contact Name | Contact Assignment |
|-------------------|---|
| NVCC_CSI | J13, J14 |
| NVCC_DRYICE | W11 |
| NVCC_EMI1 | G6, G7, G8, G9, H6, H7, H8, J6, J7 |
| NVCC_EMI2 | G12, G13, G14, G15, H12, H13, H14 |
| NVCC_JTAG | U10 |
| NVCC_LCDC | P6, P7, R6, R7 |
| NVCC_MISC | N5, N6, N7 |
| NVCC_NFC | L6, L7, L8 |
| NVCC_SDIO | R17 |
| OSC24M_GND | W15 |
| OSC24M_VDD | W16 |
| QGND | A1, A11, A20, B11, C11, D11, E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, E15, E16, F5, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, F16, G5, G10, G16, H5, H9, H10, H11, H15, H16, J5, J9, J10, J11, J15, J16, K1, K2, K3, K4, K5, K8, K9, K10, K11, K13, K14, K15, L5, L9, L10, L11, L12, L13, L14, L15, M8, M9, M10, M11, M12, M13, M14, M15, N9, N12, N13, N15, N16, P5, P13, P14, P15, P16, R5, R8, R9, R10, R11, R12, R13, R14, R15, R16, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, Y1, Y20 |
| QVDD | G11, J8, J12, K6, K7, K12, M5, M6, M7, N8, P8, P9 |
| REF | V11 |
| UPLL_GND | M16 |
| UPLL_VDD | L16 |
| USBPHY1_UPLLVD | M17 |
| USBPHY1_UPLLVS | N17 |
| USBPHY1_VDDA | K16 |
| USBPHY1_VDDA_BIAS | K19 |
| USBPHY1_VSSA | L19 |
| USBPHY1_VSSA_BIAS | J17 |
| USBPHY2_VDD | W18 |
| USBPHY2_VSS | W17 |

4.3 Signal Contact Assignments—17x17mm, 0.8mm Pitch

Table 96 lists the i.MX25 signal contact assignments.

Table 96. i.MX25 Signal Contact Assignment

| Signal Name | Contact Assignment | Signal Name | Contact Assignment | Signal Name | Contact Assignment |
|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| A0 | A18 | NFWE_B | G4 | SD1_CMD | K20 |
| A1 | B17 | NFRE_B | C1 | SD1_CLK | M20 |
| A2 | C17 | NFALE | F4 | SD1_DATA0 | L20 |
| A3 | B18 | NFCLE | E4 | SD1_DATA1 | N20 |
| A4 | C20 | NFWP_B | H4 | SD1_DATA2 | M19 |
| A5 | A19 | NFRB | C2 | SD1_DATA3 | J20 |
| A6 | C19 | D15 | J2 | KPP_ROW0 | N4 |
| A7 | B19 | D14 | J1 | KPP_ROW1 | R1 |
| A8 | D18 | D13 | H2 | KPP_ROW2 | P3 |
| A9 | C18 | D12 | H3 | KPP_ROW3 | P2 |
| A10 | A2 | D11 | F1 | KPP_COL0 | P1 |
| MA10 | D16 | D10 | F2 | KPP_COL1 | N3 |
| A11 | D20 | D9 | D1 | KPP_COL2 | N2 |
| A12 | D17 | D8 | E2 | KPP_COL3 | N1 |
| A13 | D19 | D7 | J3 | FEC_MDC | L1 |
| A14 | A3 | D6 | H1 | FEC_MDIO | L2 |
| A15 | B4 | D5 | G1 | FEC_TDATA0 | L3 |
| A16 | C6 | D4 | G2 | FEC_TDATA1 | J4 |
| A17 | B5 | D3 | G3 | FEC_TX_EN | M2 |
| A18 | D7 | D2 | E1 | FEC_RDATA0 | M1 |
| A19 | A4 | D1 | F3 | FEC_RDATA1 | M4 |
| A20 | B6 | D0 | E3 | FEC_RX_DV | M3 |
| A21 | C7 | LD0 | Y7 | FEC_TX_CLK | L4 |
| A22 | A5 | LD1 | V8 | RTCK | W10 |
| A23 | A6 | LD2 | W7 | TCK | V10 |
| A24 | B7 | LD3 | U8 | TMS | Y9 |
| A25 | A7 | LD4 | Y6 | TDI | W9 |
| SD0 | A12 | LD5 | V7 | TDO | Y8 |
| SD1 | C13 | LD6 | W6 | TRSTB | V9 |
| SD2 | B13 | LD7 | Y5 | DE_B | W8 |
| SD3 | D14 | LD8 | V6 | SJC_MOD | U9 |

Table 96. i.MX25 Signal Contact Assignment (continued)

| Signal Name | Contact Assignment | Signal Name | Contact Assignment | Signal Name | Contact Assignment |
|-------------|--------------------|-------------|--------------------|--------------|--------------------|
| SD4 | D13 | LD9 | W5 | USBPHY1_VBUS | K17 |
| SD5 | A13 | LD10 | Y4 | USBPHY1_DP | L18 |
| SD6 | D12 | LD11 | Y3 | USBPHY1_DM | K18 |
| SD7 | A10 | LD12 | V5 | USBPHY1_UID | J18 |
| SD8 | B9 | LD13 | W4 | USBPHY1_RREF | L17 |
| SD9 | D10 | LD14 | V4 | USBPHY2_DM | Y19 |
| SD10 | B10 | LD15 | W3 | USBPHY2_DP | Y18 |
| SD11 | C10 | HSYNC | U7 | GPIO_A | N19 |
| SD12 | C9 | VSYNC | U6 | GPIO_B | N18 |
| SD13 | A9 | LSCLK | U5 | GPIO_C | P17 |
| SD14 | D9 | OE_ACD | V3 | GPIO_D | P19 |
| SD15 | A8 | CONTRAST | U4 | GPIO_E | P18 |
| SDBA1 | A16 | PWM | W2 | GPIO_F | R19 |
| SDBA0 | B15 | CSI_D2 | F18 | EXT_ARMCLK | R20 |
| DQM0 | C12 | CSI_D3 | E19 | UPLL_BYPCLK | U20 |
| DQM1 | C8 | CSI_D4 | F19 | VSTBY_REQ | R18 |
| RAS | C14 | CSI_D5 | G18 | VSTBY_ACK | T20 |
| CAS | C16 | CSI_D6 | E20 | POWER_FAIL | T19 |
| SDWE | A15 | CSI_D7 | E18 | RESET_B | T18 |
| SDCKE0 | D15 | CSI_D8 | G19 | POR_B | U19 |
| SDCKE1 | C15 | CSI_D9 | F20 | CLKO | V20 |
| SDCLK | B14 | CSI_MCLK | H18 | BOOT_MODE0 | V19 |
| SDCLK_B | A14 | CSI_VSYNC | G20 | BOOT_MODE1 | W20 |
| SDQS0 | B12 | CSI_HSYNC | H19 | CLK_SEL | W19 |
| SDQS1 | B8 | CSI_PIXCLK | H20 | TEST_MODE | V18 |
| EB0 | B3 | I2C1_CLK | F17 | OSC24M_EXTAL | Y15 |
| EB1 | C5 | I2C1_DAT | G17 | OSC24M_XTAL | Y16 |
| OE | D6 | CSPI1_MOSI | T4 | OSC32K_EXTAL | Y11 |
| CS0 | C3 | CSPI1_MISO | W1 | OSC32K_XTAL | Y10 |
| CS1 | D3 | CSPI1_SS0 | R4 | TAMPER_A | N10 |
| CS2 | B16 | CSPI1_SS1 | V2 | TAMPER_B | N11 |
| CS3 | A17 | CSPI1_SCLK | U3 | MESH_C | P11 |
| CS4 | D5 | CSPI1_RDY | V1 | MESH_D | P12 |
| CS5 | D4 | UART1_RXD | U2 | OSC_BYP | Y12 |

Table 96. i.MX25 Signal Contact Assignment (continued)

| Signal Name | Contact Assignment | Signal Name | Contact Assignment | Signal Name | Contact Assignment |
|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| NF_CE0 | D2 | UART1_TXD | U1 | XP | V14 |
| ECB | B2 | UART1_RTS | T3 | XN | U13 |
| LBA | B1 | UART1_CTS | T2 | YP | V13 |
| BCLK | D8 | UART2_RXD | P4 | YN | W12 |
| RW | C4 | UART2_TXD | T1 | WIPER | U14 |
| | | UART2_RTS | R3 | INAUX0 | U11 |
| | | UART2_CTS | R2 | INAUX1 | V12 |
| | | | | INAUX2 | U12 |

Table 97 lists the i.MX25 no connect contact assignments.

Table 97. i.MX25 No Connect Contact Assignments

| Signal Name | Contact Assignment |
|-------------|--------------------|
| NC_BGA_B20 | B20 |
| NC_BGA_E17 | E17 |
| NC_BGA_H17 | H17 |
| NC_BGA_J19 | J19 |
| NC_BGA_M18 | M18 |
| NC_BGA_P20 | P20 |
| NC_BGA_U15 | U15 |
| NC_BGA_U16 | U16 |
| NC_BGA_V15 | V15 |
| NC_BGA_V16 | V16 |
| NC_BGA_V17 | V17 |
| NC_BGA_W14 | W14 |
| NC_BGA_Y2 | Y2 |
| NC_BGA_Y14 | Y14 |
| NC_BGA_Y17 | Y17 |

4.4 i.MX25 Ball Map

Table 98 shows the i.MX25 ball map.

Table 98. i.MX25 Ball Map

| | A | B | C | D | E | F | G | H | J |
|----|---------|------------|--------|--------|------------|----------|-----------|------------|-------------------|
| 20 | QGND | NC_BGA_B20 | A4 | A11 | CS1_D6 | CS1_D9 | CS1_VSYNC | CS1_PIXCLK | SD1_DATA3 |
| 19 | A5 | A7 | A6 | A13 | CS1_D3 | CS1_D4 | CS1_D8 | CS1_HSYNC | NC_BGA_J19 |
| 18 | A0 | A3 | A9 | A8 | CS1_D7 | CS1_D2 | CS1_D5 | CS1_MCLK | USBPHY1_UID |
| 17 | CS3 | A1 | A2 | A12 | NC_BGA_E17 | I2C1_CLK | I2C1_DAT | NC_BGA_H17 | USBPHY1_VSSA_BIAS |
| 16 | SDBA1 | CS2 | CAS | MA10 | QGND | QGND | QGND | QGND | QGND |
| 15 | SDWE | SDBA0 | SDCKE1 | SDCKE0 | QGND | QGND | NVCC_EMI2 | QGND | QGND |
| 14 | SDCLK_B | SDCLK | PAS | SD3 | QGND | QGND | NVCC_EMI2 | NVCC_EMI2 | NVCC_CSI |
| 13 | SD5 | SD2 | SD1 | SD4 | QGND | QGND | NVCC_EMI2 | NVCC_EMI2 | NVCC_CSI |
| 12 | SD0 | SDQS0 | DQM0 | SD6 | QGND | QGND | NVCC_EMI2 | NVCC_EMI2 | QVDD |
| 11 | QGND | QGND | QGND | QGND | QGND | QGND | QVDD | QGND | QGND |
| 10 | SD7 | SD10 | SD11 | SD9 | QGND | QGND | QGND | QGND | QGND |
| 9 | SD13 | SD8 | SD12 | SD14 | QGND | QGND | NVCC_EMI1 | QGND | QGND |
| 8 | SD15 | SDQS1 | DQM1 | BCLK | QGND | QGND | NVCC_EMI1 | NVCC_EMI1 | QVDD |
| 7 | A25 | A24 | A21 | A18 | QGND | QGND | NVCC_EMI1 | NVCC_EMI1 | NVCC_EMI1 |
| 6 | A23 | A20 | A16 | OE | QGND | QGND | NVCC_EMI1 | NVCC_EMI1 | NVCC_EMI1 |
| 5 | A22 | A17 | EB1 | CS4 | QGND | QGND | QGND | QGND | QGND |
| 4 | A19 | A15 | RW | CS5 | NFCLE | NFALE | NFWE_B | NFWP_B | FEC_TDATA1 |
| 3 | A14 | EB0 | CS0 | CS1 | D0 | D1 | D3 | D12 | D7 |
| 2 | A10 | ECB | NFRB | NF_CE0 | D8 | D10 | D4 | D13 | D15 |
| 1 | QGND | LBA | NFRE_B | D9 | D2 | D11 | D5 | D6 | D14 |

Table 98. i.MX25 Ball Map (continued)

| | | | | | | | |
|----|-------------------|--------------|----------------|-----------------|------------|------------|------------|
| 20 | SD1_CMD | SD1_DATA0 | SD1_CLK | SD1_DATA1 | NC_BGA_P20 | EXT_ARMCLK | VSTBY_ACK |
| 19 | USBPHY1_VDDA_BIAS | USBPHY1_VSSA | SD1_DATA2 | GPIO_A | GPIO_D | GPIO_F | POWER_FAIL |
| 18 | USBPHY1_DM | USBPHY1_DP | NC_BGA_M18 | GPIO_B | GPIO_E | VSTBY_REQ | RESET_B |
| 17 | USBPHY1_VBUS | USBPHY1_RREF | USBPHY1_UPLLVD | USBPHY1_UPLLVSS | GPIO_C | NVCC_SDIO | FUSE_VDD |
| 16 | USBPHY1_VDDA | UPLL_VDD | UPLL_GND | QGND | QGND | QGND | QGND |
| 15 | QGND | QGND | QGND | QGND | QGND | QGND | QGND |
| 14 | QGND | QGND | QGND | NVCC_CRM | QGND | QGND | QGND |
| 13 | QGND | QGND | QGND | QGND | QGND | QGND | QGND |
| 12 | QVDD | QGND | QGND | QGND | MESH_D | QGND | QGND |
| 11 | QGND | QGND | QGND | TAMPER_B | MESH_C | QGND | QGND |
| 10 | QGND | QGND | QGND | TAMPER_A | BAT_VDD | QGND | QGND |
| 9 | QGND | QGND | QGND | QGND | QVDD | QGND | QGND |
| 8 | QGND | NVCC_NFC | QGND | QVDD | QVDD | QGND | QGND |
| 7 | QVDD | NVCC_NFC | QVDD | NVCC_MISC | NVCC_LCDC | NVCC_LCDC | QGND |
| 6 | QVDD | NVCC_NFC | QVDD | NVCC_MISC | NVCC_LCDC | NVCC_LCDC | QGND |
| 5 | QGND | QGND | QVDD | NVCC_MISC | QGND | QGND | QGND |
| 4 | QGND | FEC_TX_CLK | FEC_RDATA1 | KPP_ROW0 | UART2_RXD | CSP11_SS0 | CSP11_MOSI |
| 3 | QGND | FEC_TDATA0 | FEC_RX_DV | KPP_COL1 | KPP_ROW2 | UART2_RTS | UART1_RTS |
| 2 | QGND | FEC_MDIO | FEC_TX_EN | KPP_COL2 | KPP_ROW3 | UART2_CTS | UART1_CTS |
| 1 | QGND | FEC_MDC | FEC_RDATA0 | KPP_COL3 | KPP_COL0 | KPP_ROW1 | UART2_TXD |
| | K | L | M | N | P | R | T |

Table 98. i.MX25 Ball Map (continued)

| | | | | |
|----|-------------|------------|-------------|--------------|
| 20 | UPLL_BYPCLK | CLKO | BOOT_MODE1 | QGND |
| 19 | POR_B | BOOT_MODE0 | CLK_SEL | USBPHY2_DM |
| 18 | MPLL_VDD | TEST_MODE | USBPHY2_VDD | USBPHY2_DP |
| 17 | MPLL_GND | NC_BGA_V17 | USBPHY2_VSS | NC_BGA_Y17 |
| 16 | NC_BGA_U16 | NC_BGA_V16 | OSC24M_VDD | OSC24M_XTAL |
| 15 | NC_BGA_U15 | NC_BGA_V15 | OSC24M_GND | OSC24M_EXTAL |
| 14 | WIPEP | XP | NC_BGA_W14 | NC_BGA_Y14 |
| 13 | XN | YP | NVCC_ADC | NGND_ADC |
| 12 | INAUX2 | INAUX1 | YN | OSC_BYP |
| 11 | INAUX0 | REF | NVCC_DRYICE | OSC32K_EXTAL |
| 10 | NVCC_JTAG | TCK | RTCK | OSC32K_XTAL |
| 9 | SJC_MOD | TRSTB | TDI | TMS |
| 8 | LD3 | LD1 | DE_B | TDO |
| 7 | HSYNC | LD5 | LD2 | LD0 |
| 6 | VSYNC | LD8 | LD6 | LD4 |
| 5 | LSCLK | LD12 | LD9 | LD7 |
| 4 | CONTRAST | LD14 | LD13 | LD10 |
| 3 | CSP11_SCLK | OE_ACD | LD15 | LD11 |
| 2 | UART1_RXD | CSP11_SS1 | PWM | NC_BGA_Y2 |
| 1 | UART1_TXD | CSP11_RDY | CSP11_MISO | QGND |
| | U | V | W | Y |

5 Revision History

Table 99 summarizes revisions to this document.

Table 99. Revision History

| Rev. | Date | Revision |
|------|--------|------------------|
| 0 | 6/2009 | Initial release. |

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